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(54) Image data processing apparatus.

(57) A video data processing apparatus converts one of NTSC type and VGA type video signals to the other or overlays the two types of video signals and outputs them as either an NTSC type overlaid video signal or a VGA type overlaid video sigal. The processing apparatus has two video memories (156, 174) for storing video signal data. One of the two video memories stores solely VGA type video data. The other video memory stores either VGA type video data or NTSC type video data depending upon the particular function being carried out by the processing apparatus. Video data may be read out from the other video memory using different scan rates so that an individually dedicated memory is not required for each type of video data in performing the above-mentioned conversions and overlays.

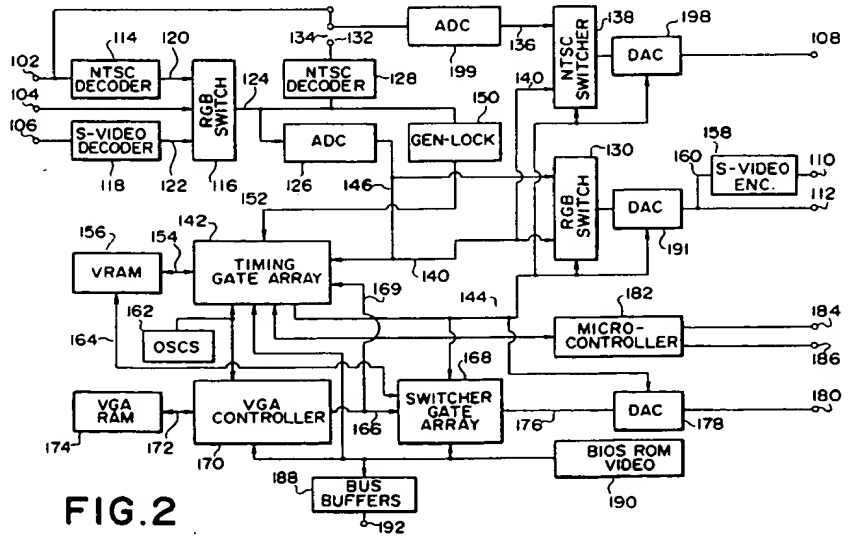

FIG.2

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an apparatus for mixing image signals and, more particularly, to an apparatus for mixing a signal representative of a graphics image generated by a computer and a video signal, such as an NTSC signal or the like, representative of a real image. The invention also relates to an apparatus for converting a signal representative of a graphics image into a video signal representative of a real image and vice versa.

Specifically, the invention relates to a memory arrangement in such an apparatus.

Description of the Prior Art

Imaging systems available today include one in which, for example, a television (TV) signal generated by a TV camera or a video signal recorded on a video floppy disc by an electronic still camera is inputted to a computer system to be displayed on a monitor in a particular form such as, for example, a video Graphics Array (VGA) form. This prior art imaging system as shown in Fig. 7 includes a personal computer 10 and an image recording and reproducing device 12 which are interfaced to each other by an electronics board 97. When the recording and reproducing device 12 is loaded with a video floppy disc 18 to read a video signal representative of a real image, the video signal is transformed into coresponding digital data by an analog-to-digital converter 98 of electronics board 97 and then developed as bit-mapped data in a dedicated video frame memory 99 also included in the electronics board. The personal computer 10 may then fetch the bit-mapped data later as needed and, thereafter, handle the data as a VGA image including displaying the data on VGA monitor 16.

Also, graphics in a VGA format generated by a personal computer may be converted to video signals capable of being recorded on a video floppy disc by an electronic still camera using conventional techniques as shown in Fig. 6. In Fig. 6, PC graphics are stored in a dedicated Buffer 1 and are read out by scan converter 2 along line 3 using a read-out rate dependent on the particular type of video signal format desired. In the figure an NTSC video signal capable of being recorded on a video floppy disc is shown as an output of scan conveter 2. However, different scan rates, for examale, PAL or SECAM scan rates, may also be used. The resultant NTSC signal in the figure may then be displayed on NTSC monitor 24.

As shown in Figs. 6 and 7, it is known to provide a conversion from VGA to NTSC and vice versa. However, using the circuits of Figs. 6 and 7, separate and independent hardware is required to store the video signal in its present state before it is converted. For example, in Fig. 6 a dedicated PC Graphics Buffer 1 must be provided to store the VGA signal before it is converted to NTSC by scan converter 2 since the VGA data must be arranged in a predetermined way so that the fixed rate scan converter 2 may properly access it in order to transform the signal to NTSC. Likewise, in Fig. 7 a dedicated frame memory 99 must be provided to store an NTSC signal before it is converted to VGA by the fixed-rate read-out operation of personal computer 10. Therefore, a large amount of hardware is needed in order to convert NTSC video signals to VGA and vice versa.

It is also known to insert (overlay) a computer graphics (VGA) signal in selected locations of an NTSC image and to display the thus-combined video signal onto an NTSC monitor such as a conventional TV receiver. Such a conventional system is shown in Fig. 8. An interlaced NTSC video signal is input to input terminal 202 and supplied to video combiner 203. A synchronization component of the input NTSC video signal is supplied to Gen-lock circuitry 201 which provides an output to video format converter 200. Non-interlaced VGA signals are pre-stored in PC graphics memory 100 and are supplied to scan-rate converter 200 which modifies the scan rate of the input non-interlaced VGA signals based on the output of the Gen-lock circuitry 201. The Gen-lock circuitry 201 receives the synchronization component of an input video signal, in this case NTSC, and provides an output to video format converter 200 so that the converter 200 can modify the format of its input, in this case VGA from PC graphics memory 100, so that the output of the converter 200 has a format equal to the input signal to the Gen-lock circuitry 201.

In Fig. 8 the converter 200 modifies the non-interlaced VGA input into interlaced VGA in the NTSC format and supplies the interlaced VGA to Video combiner 203. At this point the VGA signal is of the same format (i.e., interlaced) as the NTSC video signal which is also supplied to video combiner 203. The output 204 of combiner 203 is an interlaced VGA signal overlaid onto an NTSC signal.

It is also known to overlay NTSC video signals onto VGA signals and to display the result onto a VGA monitor using prior art systems. However, a dedicated VGA Buffer and a dedicated NTSC video memory are required in the prior art systems.

As is clear from the description of the prior art systems above, a separete and dedicated frame memory or Buffer is required to hold each type of

image signal, since a different type of image signal has a different format (i.e., interlaced or non-interlaced). For example, in Fig. 7 a separate dedicated frame memory 99 is required to store the NTSC signal before it is converted to VGA. Further, a separate and dedicated PC Graphics buffer (1,100) is required in Figs. 6 and 8, respectively, in order to store VGA signals.

Since dedicated Buffers or memories have been required by the prior art, a large amount of hardware is necessary in order to provide image signal processing equipment capable of handling a variety of image signal formats.

As described above, imaging systems available today include one in which, for example, a television (TV) signal generated by a TV camera and a video signal recorded in a video floppy by an electronic still camera are inputted to a computer system to be displayed on a monitor in a particular from such as a Video Graphics Array (VGA) image. This prior art imaging system includes a personal computer and an image recording and reproducing device which are interfaced to each other by an electronics board. For example, when the recording and reproducing device is loaded with a video floppy to read a video signal representative of a real image, the video signal is transformed into corresponding digital data by the electronics board and then developed as bit-mapped data in a video memory included in the electronics board. The personal computer may fetch the bit-mapped data later as needed and, thereafter, handle then as VGA image or a part thereof.

The conventional system in which a personal computer and an apparatus for recording and reproducing images from a video floppy are combined allows video data to be transferred from the recording and reproducing apparatus to the personal computer, it does not allow the transfer thereof from the personal computer to the recording and reproducing apparatus. Specifically, with such a system, it is impossible to read a real image out of a video floppy, process it in the personal computer, and then write the processed image again to the video floppy.

With the increasing spread of computer systems and video systems, there is an increasing demand among users for an implementation which makes the most of various merits available with the combination of the two different systems. For example, it is often desired to see the contents of images stored in a video floppy, video tape or similar image recording medium instantaneously in a summarized image. It is also desired to add a title or bibliographic item to such a summarized image and then write the result back to the same recording medium.

In the above-mentioned system, video output signals representing a mixture of a computer graphics (VGA) image and an NTSC-type image are easily displayed on a selected one of a computer graphics (VGA) type monitor or am NTSC-type monitor. However, the combined (overlaid) video image signals are not so easily sent on to an external memory. Difficulties arise in attempting to store an overlaid video signal in an external memory because the speed of the overlaid signal as it comes out of the above-mentioned video processing system is too fast for an external memory to handle. For example, the overlaid signals are sent out at a rate in the Megahertz (MHz) region. It would be useful to be able to store overlaid images in an external memory as an alternative to merely displaying the overlaid image onto a monitor display. By storing overlaid images in an external memory they would be able to be easily and selectably read out and displaced on a monitor at a later time without having to re-overlay the image signals making up the composite overlaid signal. Also, further processing or overlaying of the overlaid signals would be simplified.

A video signal processing apparatus has been described in a co-pending application entitled "Video Processing System Memory for Storing a Variety of Video Signal Formats" and filed in the name of the same applicant as that of the present application and involves a system for converting one of NTSC type and VGA type video signals to the other or overlays the two types of video signals and outputs them as either an NTSC type overlaid video signal or a VGA type overlaid video signal. The processing system has two video memories storing video signal data. One of the two video memories stores solely VGA type video data. The other video memory stores either VGA type video data or NTSC type video data depending upon the particular function being carried out by the processing system. Video data may be read out from the other video memory using different scan rates so that an individually dedicated memory is not required for each type of video data in performing the above-mentioned conversions and overlays.

In the above-mentioned system, however, the video signal output of the overlay and rescan board can only be sent to one type of moniter, the monitor capable of handling the scan rate of the board's output video signal.

NTSC-type video signals exist in an interlaced format where the scan lines of one of two fields of a frame of video data are displayed on a monitor and the scan lines of the other field are interlaced between the scan lines of the first field. The interlacing effect makes a signal easier to view from a large distance since glare is reduced by dispensing local intensities within a signal. If this interlaced

display is viewed from a close-up distance, for example, in small audience situations, the interlacing of the scan lines produces a visible jitter effect which is unpleasant to the eye. If the interlaced display is viewed from a large distance, for example, in large audience situations, the jitter effect is less noticeable.

VGA-type video signals exist in a non-interlaced format. This type of display is meant to be observed at a close-up distance, for example, a couple of feet away in computer monitor environments. Since the VGA-type monitor is non-interlaced, the above-mentioned effect of jitter is not observed. However, due to the non-interlacing of scan lines, the monitor is difficult to view from a distance due to glare produced by concentrated local intensities within a signal.

Based on the above discussion, it is clear that an interlaced display is ideal for large distance, for example, large audience situations, and that a non-interlaced display is ideal for small distance, for example, small audience situations. Therefore, it would be useful to provide for a video signal processing system where it is possible to provide a video signal output on either an NTSC-type monitor or a VGA-type monitor.

SUMMARY OF THE INVENTION

An object of the present invention is to provide image signal processing equipment capable of handling a variety of image signal formats.

It is a further object of the invention to provide an image signal processing system capable of handling a variety of image signal formats and using a minimum amount of hardware so as to reduce costs of the overall system.

The above objects have been attained by the inventors by providing an improved image overlay and rescan board capable of receiving image signals of a variety of formats including NTSC image signals representative of a real image and VGA image signals representative of a computer generated graphics image. The overlay and rescan board includes a timing gate-array for addressing a frame memory and for sending and receiving data to and from the frame memory.

Both image signals representative of a real image and image signals representative of a computer generated graphics image are capable of being selectively received by and sent to the timing gate-array depending on the particular type of operation to be performed by the overlay and rescan board. Possible operation of the board include conversion from computer graphics image signals to image signals representative of real image (such as NTSC video) and vice versa, and overlaying of computer graphics image signals onto image signals representative of real images and vice versa.

Depending on the particular operation to be carried out by the overlay and rescan board, the timing gate-array either reads from or writes to the frame memory at a read/write rate dependent on the type of image signal to be read from or written to the frame memory.

In this way, a single frame memory is capable of temporarily storing an image signal of either a computer graphics type or a real image type. Thus, an overlay and rescan board capable of performing a variety of image processing operations having a minimum amount of hardware is achieved.

A still further object of the present invention is to provide a video signal processing apparatus in which an overlaid signal may be simultaneously displayed on either an NTSC-type monitor or a VGA-type monitor.

The last-mentioned object is achieved by providing a video processing apparatus in which an NTSC-type video signal is overlaid onto a VGA-type signal as described above, and futher, the overlaid signal is fed to a line buffer which performs scan conversion the overlaid signal The scan-converted overlaid signal, which has been either scan-converted to the RGB or NTSC formats, is next displayed on either an RGB or NTSC, respectively, monitor.

A still further object of the invention is to provide a video image processing system in which overlaid image signals, obtained by overlaying VGA-type image signals onto NTSC-type video signals or vice versa, may be easily stored to an external memory.

The last-mentioned object has been attained by placing a feedback connection from an output of a video image switcher, used to combine two signals making up the composite overlaid signal, back to an input of control means used to control the write in/read out rate of an internal frame memory. The overlaid image, once formed, is fed back to the control means and stored into the internal frame memory. Once the overlaid image has been stored in the internal frame memory it may easily by read out and stored into an external memory at a transfer rate which the external memory can handle, i.e., a transfer rate substantially less than the Megahertz (MHz) range rate at which the overlaid images are provided.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the present invention will become more apparent from the consideration of the following detailed description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram schematically showing a preferred embodiment of the video signal mixing apparatus in accordance with the present invention;

Fig. 2 is a schematic block diagram showing a specific construction of an overlay and rescan board included in the illustrative embodiment;

Figs. 3 and 4 each show a specific image which may be produced by the illustrative embodiment;

Fig. 5 shows a specific format of video data applicable to the illustrative embodiment;

Fig. 6 shows a conventional system for converting VGA signals to NTSC image signals;

Fig. 7 shows a conventional system for converting NTSC to VGA image signals;

Fig. 8 shows a conventional system for overlaying VGA onto NTSC image signals;

Figs. 9 and 10 each show a schematic block diagram of a specific construction of an timing gate-array included in the illustrative embodiment;

Fig. 11 shows a switcher gate-array of the illustrative embodiment;

Fig. 12 shows a flow chart for explaining the operation of the switcher gate-array of the illustrative embodiment;

Figs. 13 and 14 each show a specific index image data which may be produced by the illustrative embodiment;

Fig. 15 is a schematic block diagram showing a specific construction of an overlay and rescan board included in the alternative embodiment; and

Fig. 16 is a schematic block diagram showing a specific construction of an overlay and rescan board included in another alternative embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1 of the drawings, a video or image signal mixing apparatus embodying the present invention is shown and has a personal computer 10 and a rec/player 12 which are interconnected by an overlay and rescan board 14. The personal computer 10 is a commercially available 16-bit or 32-bit processor system and includes program sequences for handling graphics and text. Advantageously, the personal computer 10 may be implemented with a processing system corresponding to IBM PC/XT/AT to SP/2 M-30, for example. Graphics data are dealt with as raster date, vector data, or bit-mapped data. A VGA monitor 16 is connected to the computer 10 and, in the illustrative embodiment, visibly displays VGA video data rendered in a pseudo-color mode. A VGA image has a standardized screen size and is non-interlaced, as is well known in the art. In general, VGA image data are represented in a pseudo-color mode where one pixel of image data is represented by one numerical value, as is also known in the art. When a look-up table is referenced with the numerical value being used as an address, a group of three color components associated with the numerical value is produced. This group of color components determines the color and luminace of the pixel of interest.

The rec/player 12 is a recording and reproducing unit for writing a true-color mode analog video signal to a video floppy 18 and reading it out of the video floppy 18. A video signal source such as a high resolution camera 20 is also connected to the rec/player 12. The rec/player 12 may be of the type having a function of recording and reproducing a video signal to and from a video tape, not shown, in place of or in addition to the video floppy 18. Generally, a TV signal or similar signal-representative of a real image produces colors and luminance in a true-color mode where one pixel is represented by three numbers representing the weights of three color components, red, green, and blue, so that the reproduced image is impressive to some degree.

An overlay and rescan board 14 connects the personal computer 10 and rec/player 12 to each other. In the illustrative embodiment, the board 14 has a signal converting and mixing function, i.e., it is capable of receiving NTSC, RGB and S-type video signals, as well as VGA video signals and outputting them as any one of NTSC, RGB, S-type and VGA video signals as needed. Fig. 2 shows a specific construction of the overlay and rescan board. It should be kept in mind that the present invention is advantageously practicable not only with the above-mentioned types of video signals but also with other types of video signals such as PAL and SECAM.

The overlay and rescan board 14 has input ports 102, 104 and 106 for receiving video signals representative of real images, and output ports 108, 110 and 112 for outputting video signals representative ofreal images. The input ports 102, 104 and 106 are individually connected to any desired video signal sources such as the high resolution camera 20, a player for playing the video floppy 18 or a video tape, an image scanner, or a communication line, not shown. The output ports 108, 110

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and 112 constitute a part of the connection line of the board 14 to the rec/player 12 and are connected to the drive of the video floppy 18 or a video tape, not shown, and/or a video monitor 24, and other similar picture output units.

The input port 102 receives an NTSC signal and is connected to the input of an NTSC decoder 114 which transforms an NTSC video input on the input 102 into an RGB video signal and feeds the RGB video signal to an input 120 of an RGB swith 116. The input port 104 receives an RGB signal and feeds it directly to the RGB switch 116, while the input port 106 receives an S-type video signal and applies it to the input of an S-video decode 118. The S-video decoder 118 transforms the video input on the input 106 into an RGB video signal and delivers the resulting signal to another input 122 of the RGB switch 116. It will be seen that in the illustrative embodiment the overlay and rescan board 14 handles videosignals basically as RGB signals.

The RGB switch 116 plays the role of a selector circuit for selectively connecting the three inputs 120, 104 and 122 to an output 124 thereof one at a time. The output 124 of the RGB switch 116 is connected to the inputof an analog-to-digital converter (ADC) 126, an NTSC encoder 128, and a Gen-lock circuit 150. The NTSC encoder 128 converts the RGB signal on the input 124 into an NTSC signal and then feeds it out via an output 132 thereof. The output 132 is connected to a selector circuit 134. Also connected to the selector circuit 134 is the direct NTSC input 102. The selector circuit 134 selectively connects either one of the two NTSC inputs 102 and 132 to an A/D converter 199 which has an output 136 thereof which is connected to one input of an NTSC switcher 138. The NTSC switcher 138 has two inputs 136 and 140 an output connecting to the video output 108 through a digital-to-analog converter 198. The NTSC switcher 138 selectively connects either one of the two inputs 136 and 140 to the output 108 in respons to a control output 144 which is fed thereto from a timing gate-array 142, as will be described specifically later. This switching operation of the swithcher 138 can be implemented with the pixel clock rate.

The ADC 126 has a reference generator, not shown, for setting a full scale range and coverts an analog RGB signal appearing on the input 124 into corresponding digital data, the digital data being fed out via an output 146. The output 146 is connected to the timing gate-array 142. The output 124 of the RGB switch 116 is connected to a Gen-lock circuit 150 also. The Gen-lock circuit 150 locks its output signal phase to the video frequency of the input 124 and generates a high-speed clock meant for the other logic circuitry on an output 152 thereof. The output 152 is connected to the timing gate-array 142.

The timing gate-array 142 is a programmble video timing generator, which generates video synchronisation signals for virtually any type of video in response to reference clocks generated by reference oscillators 162. As an example, two popular video standards are NTSC and VGA. Both of the two video standards have different characteristics. Conventionally, equipment which is designed for one standard could not be used with theother. As a result, it is useful for a video product to provide both types of output. Historically, such products utilize one frame memory to generate NTSC, and another frame Buffer to generate VGA. The present invention relies on the fact that many applications need not generate both simultaneously, and by using a programmable frame memory only one frame memory is required.

In the illustrative embodiment, the timing gate-array 142 is so constructed by hardware as to be capable of selectively writing either one of NTSC type video signals and VGA video signals to a video RAM (VRAM) 156 and reading out the signals stored therein. The VRAM 156 and timing gate-array 142, therfore, constitute a programmable frame memory, and this memory implements scan conversion. Specifically, with the programmable frame memory it is possible to transform VGA type video signals into NTSC type video signals and vice versa.

The timing gate-array 142 has a data input/output port 154 which is connected to the VRAM 156. The VRAM 156 is a RAM capable of storing video data having various video formats and, in the illustrative embodiment, has a capacity great enough to accommodate one frame of video data, i.e., 1 Mbyte. The timing gate-array 142 and VRAM 156 together form a programmble video image generator.

The details of the timing gate-array 142 are clearly shown in Figs. 9 and 10 which will be explained now. Gen-lock logic block 713, shown in Fig. 10 receives video synchronization information derived from the signal output from RGB switch 116, shown in Fig. 2, by way of the Gem-lock circuit 150 along line 152. The video synchronization information could pertain to either RGB, NTSC or S-type video depending on the particular signal output from the RGB swith 116. The video synchronization information is next sent through a programmble sync generator 712, which will be described below, and on to a VRAM address Buffer/Multiplexer 703, shown in Fig. 10 which will also be described below.

The Gen-lock logic block 713 of the timing gate-array 142 is constantly monitoring the Gen-lock circuit 150, shown in Fig. 2, to see if the Gen-lock circuit is outputting synchronization information. When the Gen-lock logic 713 senses that Gen-lock circuit 150 is not outputting video synchronization information, Gen-lock logic 713 sends a signal to the programmable sync generator 712 to initiate a free running mode in the programmable sync generator 712. In this freerunning mode the programmable sync generator generates internal synchronization information based on information sent to the programmable sync genertor 712 by the personal computer 10 along the CPU bus 192 and along line 717. The information sent along line 717 from the personal computer 10 may include information relating to a variety of video synchronization formats, such as NTSC, PAL, S-type, or RGB, for example. The free running mode is used for situations when no external signal is sent through the RGB switch 116 to the Gen-lock circuit 150 shown in Fig. 2. Such a situation, for example, would occur during a conversion from VGA type information to NTSC type information, as will be described below.

A second programmable sync generator 711 is used for generating synchronization information relating to VGA signals. The programmable sync generator 711 receives inputs from the VGA controller 170 shown in Fig. 2 and form the CPU bus 192 for providing the sync generator 711 with the proper infomation it needs to produce synchronization information relating to the VGA format. The connection from the CPU bus 192 to the sync generator 711 through line 718 provides for the programming of the sync generator 711 during a free running mode, such as the one described above with respect to the programmable sync generator 712. During a non-free running mode the programmable sync generator 711 receives external synchronization information along line 166 from the VGA controller 170. During the free running mode, when a VGA signal is not applied to line 166, the sync generator 711 produces internal synchronization information based on information sent to the sync generator 711 along CPU bus 192 and along line 718. The information sent along line 718 may relate not only to VGA type information, but also to new types of PC graphic signals which may envole. Therefore, the programmable sync generators 711 and 712 are fully programmable so that any type of video signal synchronization format may be created.

Synchronization information from the programmable sync generators 711 and 712 is applied to the VRAM address Buffer/Multiplexer 703, shown in Fig. 9 as separate inputs. The VRAM address Buffer/Multiplexer 703 receives a plurality of inputs and selects one of the inputs so at to provide an output along line 154 to VRAM 156. The output of Buffer/Multiplexer 703 is sent to the VRAM 156 to provide read and write signals at a time dependent upon the timing of the selected synchronization signal input to the Buffer/Multiplexer 703.

The Buffer/Multiplexer 703 also receives an input from a CPU counter 705. The CPU counter 705 receives an input from the CPU bus 192 so that information from the personal computer 10 may be sent to the CPU counter 705 to specify an exact location, on a pixel-by-pixel basis, of information stored in or to be stored in the VRAM 156. The CPU connter 705, therefore, allows the personal computer 10 to randomly access the VRAM 156.

The Buffer/Multiplexer 703 is controlled by a VRAM state machine 704 along line 719. The state machine 704 receives input from the programmable sync generators 712 and 711 along limes 706 and 720, respectively. The state machine 704 receives another input along lime 721 from the CPU bus 192. By receiving these three inputs the VRAM state machine 704 is capable of monitoring the activity of the timing gate-array to decide which of the Buffer/Multiplexer 703 inputs are to be applied to the output 154. The VRAM state machine 704 also receives an input from clock Buffers 707 connected to clock oscillators 162 as shown in Fig. 2. These clock oscillators provide the VRAM state machine with basic timing signals for operating a selection process for selecting the particular input to the multiplexer 703 which is to be applied to output 154.

Video data output from RGB switch 116 via ADC 126, shown in Fig. 2, is input to the timing gate-array 142 and sent along line 140 to Buffer 714 shown in Fig. 10. The data is sent from Buffer 714 to FIFO shift register 702, shown in Fig. 9, along line 722 when data is being written from the RGB switch 116 to the VRAM 156 through the timing gate-array 142. The data is next sent to VRAM data Buffer 701 where the data is held until write commands from the VRAM address Buffer/Multiplexer 703 control the timing of the write operation of the VRAM to write therein data held in the Buffer 701. Information being read from the VRAM 156 is also sent through Buffer 701, shown Fig. 10, and FIFO 702 along line 722 and into Buffer 714 where it is output onto line 140.

VGA data from VRAM controller 170 is input, for control purposes as will be described below, to the timing gate-array 142 into the Buffer 715, shown in Fig. 10. The VGA data is also sent to the programmable sync generator 711 for Gen-locking purposes, i.e., to inform the generator 711 whether to use a sync signal supplied by the computer 10 along line 166 or to use an internal sync supplied along line 718. The VGA format stored in Buffer

715 is applied to overlay logic block 716 which receives an additional input from the CPU bus 192. The overlay logic block 716 contains an overlay color register for storing a keying color digital representation; such a keying color being, for example, the color transparent, and an actual data register for storing actual data input to the overlay logic block along line 723 from Buffer 715. The overlay logic block further includes a comparator for comparing the contents of the actual data registerand the overlay color register for pixel-by-pixel color keying according to well know overlay techniques. That is, for example, if the keying color is detected in the VGA data sent to the overlay logic block 716 or line 723, then a command signal is sent, one line 144, to the switcher gate-array 168, which will be described later, so as to command the switcher gate-array 168 to swith (key) from taking its output from the VGA RAM 174 to a situation where 168 takes it output from VRAM 156.

Fig. 10 also shows microcontroller logic block 710 which receives inputs from the clock Buffers 707 and the CPU bus 192. This microcontroller logic block is used for controlling external video disk players, or the like, along line 182 and does not form a major part of this invention.

The timing gate-array line 140 is connected to inputs of the NTSC switcher 138 and the RGB switch 130. The RGB switch 130 serves as a selector circuit for selectively outputting either one of the two inputs 124 and 140 in response to the control output 144 of the timing gate-array 142. The output of the switch 130 is connected to an input 160 of an S-video encoder 158 and the RGB format output port 112 through a digital-to-analog converter 191. The S-video encoder 158 transforms the RGB signal into an S-type video signal and outputs thelatter on an output 110 thereof.

The VRAM 156 has an additional data input/output port 164 which is connected to one input of a switcher gate-array 168. The other input/output port 166 of the switicher gate-array 168 is connected to the timing gate-array 142 and a VGA controller 170. The VGA controller 170 converts software commands into bit-mapped pixel images as is well-known in the art. The VGA controller 170 has an input/output port 172 to which a VGA RAM 174 is connected. The VGA RAM 174 stores video information having various formats generated by the personal computer 10 as is well known in the art. While the video information may be of any one of the raster type, vector type, and bit-mapped type, it is transformed into raster data before being written to the VGA RAM 174. Of course, the video information may include text data. In the illustrative embodiment, the VGA RAM 174 has a capacity of 1 Mbyte.

The switcher gate-array 168 as shown in detailin Fig. 11 is a selector circuit which delivers a video signal read from the VRAM 156 and appearing on the output line 164 to an output 176 thereof through Buffer 1001, MUX 1004 and Buffer 1005, or selectively applies a VGA video output fed thereto from the VGA RAM 174 via line 172, VGA controller 170, and line 166 to either one of output 176 through Buffer 1002, MUX 1004 and Buffer 1005 and output 164 through Buffer 1002, Buffer 1003 and Buffer 1001 to the VRAM 156, as instructed by the control output 144 of the timing gate-array 142. The output 176 of the switcher gate-array 168 is connected to a video DAC 178 which, like the video DAC 148, converts digital video data into a corresponding analog VGA signal and delivers the latter to an output 180. The output 180 is connected to the VGA monitor 16 shown in Fig. 1.

The two-to-one multiplexer (MUX) 1004 in Fig. 11 of the switcher gate-array receives a control signal form the overlay logic block 716 along line 144 so as to decide, on a pixel by pixel basis, whether data stored in VRAM 156 or data stored in VGA RAM 174 is to be selected as an MUX output. Control logic block 1007 receives control signals from the CPU bus 192 for use in controlling whether or not the loop-back path created through Buffer 1003 is operable based on desired data flow paths.

Figure 12 shows a flow chart for dascribing the operation of the switcher gate-array 168. First of all, if the computer 10 has sent a control signal to control logic block 1007 so as to enable Buffer 1003 along line 1006, (Step S1), data appearing on line 166, which comes from the VGA controller 170 and VGA RAM 174, is sent through Buffer 1002, Buffer 1003 and Buffer 1001 onto line 164 (Step S2).

If the decision in Step S1 was NO, i.e., if the computer 10 has not enabled Buffer 1003, then if the overlay logic block 716 of Figure 10 has issued a command on line 144 to indicate that the keying color, for example, transparent, has been sent to 716 from Buffer 715 (Step S3), then Step S4 is executed. If Step S4 is reached, this means that the predetermined keying color is included in the VGA data coming into the timing gate-array 142 along line 166 through Buffer 715 and on to overlay logic block 716 on line 723 of Figure 10. The presence of this keying color in the VGA data acts as a signal to stop the switcher gate-array 168 from outputting data from the VGA RAM 174 and to output a pixel of data from the VRAM 156 instead. Therfore, an overlaying effect is created.

Specifically, if at Step S3 the answer is YES then this means that overlay logic block 716 has determined that the keying color has been detected in the VGA data stream and Step S4 is

executed, wherein data from lime 164 (from VRAM 156) is sent through Buffer 1001, two-to-one MUX 1004 and Buffer 1005 and onto switcher gate-array 168 output line 176. And, if at Step S3 the answar is NO, then this means that overlay logic block 716 has determined that the keying color has not been detected in the VGA data stream and step S5 is executed, wherein data from line 166 (from VGA RAM 174) is sent through Buffer 1002, two-to-one MUX 1004 and Buffer 1005 and on to switcher gate-array 168 output line 176. Therefore, Figure 12, in conjunction with Figures 9, 10 and 11, decribes the switcher gate-array 168 operation and the role of the switcher gate-array 168 in the overlaying of NTSC-type video data onto VGA-type image data.

The switcher gate-array 168 has the capability of recognizing whether each pixel is either of the true-color or the pseudo-color format, and controls video DACs 191, 198 and 178 in the appropriate manner. As a result, the hardware can switch between true-color and pseudo-color modes on a pixel-by-pixel basis. In the illustrative embodiment, pixels are represented by 16 bits, which include a bit #15 representing the true-color or pseudo-color mode, as shown in FIG. 5. If the bit #15 is a "1", the pixel is in the true-color mode while if bit #15 is a "0", the pixel is in the pseudo-color mode. This makes it possible to have a system which uses both representations simultaneously. Various sections of a video image are representable in the true-color format, while other sections are representable in the pseudo-color format. The remaining bits #14 through #0 are used in the conventional manner, i.e., to represent image data.

On receiving video data from the ADC 126, the timing gate-array 142 adds the bit #15 representative of the true-color mode to the input data before writing it to the VRAM 156. VGA video data generated by the personal computer 10 is once written to the VGA RAM 174 via a bus192, as will be described. Then, the VGA controller 170 reads the data out of the VGA RAM 174 and transfers it to the VRAM 156 via the switcher gate-array168, while adding the bit #15 representing the pseudo-color mode to the data.

A microcontroller 182 is connected to the timing gate-array 142 and has connection lines 184 and 186 connecting to the rec/player 12 and other similar video equipment. A bus Buffer 188 and a BIOS ROM 190 are connected to the timing gate-array 142, VGA controller 170, and switcher gate-array 168. The bus Buffer 188 interfaces the overlay and rescan board 14 to the personal computer bus 192. The BIOS ROM 190 stores and provides software to support the fundamental operations of the overlay and rescan board 14.

The frame memory which is identified as VRAM 156 can be connected to various video inputs and output. It is controlled by timing gate-array 142, which can be programmed to generate memory control signals and video synchronization signals for virtually any video standard. As a result, the signals frame memory 156 can generate video for virtually any video standard. The programmable frame memory constituted by the VRAM 156 and timing gate-array 142 as stated earlier is used to generate the VGA type video signal and to generate the NTSC type video signal.

Now, a first function of the inventive overlay and rescan board will be described. This first function involves transforming VGA-type image signals to NTSC-type video signals. First, a brief description will be given of this function and immediately following will be a detailed description of the function.

VGA video data, for example, is fed from the personal computer 10 to the overlay and rescan board 14 via a bus 192. The VGA video data is once written to the VGA RAM 174 under the control of the VGA controller 170. To transform the VGA type video data into a real image type video signal, the switcher gate-array 168 causes signals from the VGA RAM 174 to be input to the VRAM 156 along lines 172, 166 and 164. As a result, the VGA video data stored in the VGA RAM 174 is read out under the control of the VGA controller 170 and then written to the VRAM 156. The timing gate-array 142 reads the video data out of the VRAM 156 in response to am NTSC, or other real image, standard timing signal generated by the Gen-lock circuit 150 while feeding the thus read-out video data to the NTSC switcher 138 or the RGB switch 130 along line 140.

By such a procedure, scan conversion from a VGA type video to an NTSC, for example, type video signal is executed. When the output of the board 14 is to be an NTSC signal, the NTSC switcher 138 connects the input 140 to the output 108 through digital-to-analog converter 198 with the result that NTSC type video signals are fed out via the output 108. When the output of the board 14 is to be an RGB signal or an S-type video signal, the RGB switch 130 selects the input 140 to cause RGB type video signals to appear on the output 112 through digital-to-analog converter 191. Concerning S-type video format, the S-video encoder 158 encodes the output of the RGB switch 130 into the S-type video format, and the S-type video signal appears on the output 110.

Now, as stated above, a detailed description of the first function, that is, transforming VGA-type signals to NTSC-type signals will be given. As shown in Figure 2, video graphics data from the computer 10 is sent along line 192 through bus

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Buffers 188 and to the VGA controller 170 where it is sent along line 172 to VGA RAM 174. The VGA RAM 174 holds the data until the data is ready to be transformed from VGA type from into NTSC type form.

The VGA data is read out of the VGA RAM 174 along line 172 by the VGA controller 170. The data is next sent along line 166 to the switcher gate-array 168 whose details are shown, as described above, in Figure 11. At this point, the computer 10 sends a control signal along line 192 to the control logic block 1007, shown in Figure 11. The control logic block 1007 next sends a command signal along line 1006 to Buffer 1003, thus enabling the Buffer. Then, the video graphics data input to the switcher gate-array 168 along line 166 is sent through Buffer 1002 and further through Buffer 1003 up to Buffer 1001. Then, the data leaves the Buffer 1001 along line 164 and, thus, leaves the switcher gate-array 168 and makes its way to the VRAM 156.

VGA timing data, included in the VGA data, is sent along line 166 and along line 169, shown in Fig. 2, from the VGA controller 170 to the timer gate-array 142. Specifically, as shown in Figure 10, the VGA timing datais applied to the programmable sync generator 711, shown in Fig. 9 where the sync signals are further sent to the VRAM address Buffer/Multiplexer 703 and the VRAM state machine 704 along lines 799 and 720, respectively. As described above, the VRAM state machine 704 controls the VRAM address Buffer/Multiplexer 703 so as to select from the plurality of inputs applied to the VRAM address Buffer/Multiplexer 703 one output to be used as address timing data during reading or writing to or from the VRAM 156. In this case, the VRAM state machine 704 receives the VGA sync information along line 720 and sends a control signal along line 719 to the VRAM address Buffer/Multiplexer 703, such a command signal telling the VRAM address Buffer/Multiplexer 703 to select input line 799 to be outputted along line 154 as write timing data for the VRAM 156.

In this way, the VGA data on lime 164 from the switcher gate-array 168 is written into the VRAM 156 using write timing information which corresponds to VGA sync information supplied along line 154 from the timing gate-array 142.

Then, the Gen-lock logic block 713 detects, as described above, that no signal is being applied there to on lime 152. This is because there is no NTSC-type signal applied along line 124 to Genlock circuitry 150 in this operation.

As a result, the programmable sync generator 712 enters a free running mode, as described above, where the computer 10 sends synchronization signals along line 192 and line 717 to the programmable sync generator 712 so as to program the generator 712. As a result, the generator 712 outputs synchronization information, according to the synchronization information applied to the generator 712 along line 717. In the described example, VGA type data is to be transformed into NTSC type data so the computer 10 sends NTSC type synchronization information along line 717 to the programmable sync generator 712. The output of the programmable sync generator 712 on line 798 goes to the VRAM address Buffer/Multiplexer 703. An output of the line programmble sync generator 712 splits off of line 798 to line 706 which goes to the VRAM state machine 704. By supplying the command signal along line 706 to the VRAM state machine 704, the VRAM state machine 704outputs a command signal 719 to the VRAM address Buffer/Multiplexer 703, thus selecting the NTSC type synchronization information along line 798 to be output onto line 154 of the VRAM address Buffer/Multiplexer 703. In this way, read information with respect to the VRAM 156 is supplied to the VRAM 156 along line 154. The VGA data stored in the VRAM 156 is thus read out of the VRAM 156 along line 154 and is applied to the VRAM data Buffer 701 and further to the FIFO circuit 702 and on to the Buffer 714 along lime 722. Once the data is in the Buffer 714, the data is applied to line 140 where it is sent, as shown in Figure 2, to the NTSC switcher138. The data is next output from the switcher 138 to the DAC 198 where it is converted into analog form and the resultant NTSC video data is available on output terminal 108.

Now, a second function of the inventive overlay and rescan board will be described, this second function involves transforming NTSC-type video data to VGA type image data. First, a brief description of this function will be presented and immediately following will be a detailed description of the function.

To convert real image type video signals into VGA type video signals, the switcher gate-array 168 connects the connection line 164 from the VRAM 156 to the output 176 which is connected to the video DAC 178. NTSC type video signals coming in through the input terminal 102 are decoded into RGB signals by the NTSC encoder 114 and then applied to the ADC 126 via the RGB switch 116. If the input signals are RGB signals, they are directly fed to the RGB switch 116 via the terminal 104. In the case of S-type video signals, they are routed through the input port 106 to the S-video encoder 118, encoded into RGB signals by the encoder 118, and then applied to the RGB switch 116. This analog RGB signal is converted by the ADC 126 into corresponding digital data, and the digital data is written to the VRAM 156 via the timing gate-array 142. In response to the VGA

timing signal, the timing gate-array 142 reads the video data out of the VRAM 156 and delivers it to the video DAC 178 via the output port 164 and switcher gate-array 168. Such a procedure implements the scan conversion of real image type video, such as NTSC, into VGA type video.

The following detailed example will be given for the second function of the invention. This example describes the transformation of an NTSC type signal into a VGA type signal. An NTSC type signal is applied on line 102 as shown in Figure 2 to an NTSC decoder 114 where the NTSC signal is transformed into an RGB signal and sent along line 120 to RGB switch 116. The signal is then output from the RGB switch 116 onto line 124 and is applied to both ADC 126 and a Gen-lock circuit 150. The Gen-lock circuit 150 takes the synchronization information from the NTSC signal and locks it, in a manner similar to a well known phase lock loop. The output of the Gen-lock circuit 150 is thus NTSC synchronization information which is sent along line 152 to the timing gate-array 142. The output of the ADC 126 is sent along line 146 and line 140 to the timing gate-array 142.

The output of the Gen-lock circuit 150, on line 152, is applied to the Gen-lock logic block 713, as shown in Figure 10. The synchronization information is then output from the Gen-lock logic block 713 and applied to the programmable sync generator 712 where the synchronization information passes through the generator 712 on line 798 and onto the VRAM address Buffer/Multiplexer 703. Also, the output of the programmable sync generator 712 is applied to line 706, which branches off line 798, and line 706 is lead to the VRAM state machine 704. The VRAM state machine 704, which has the synchronization information applied to it on line 706 thus knows that the programmable sync generator 712 wishes to gain access to the VRAM 156. Thus, the VRAM state machine causes the VRAM address Buffer multiplexer to output on line 154 the synchronization information applied to the VRAM address Buffer/Multiplexer 703 along line 798 from the programmble sync generator 712. The output of the VRAM address Buffer/Multiplexer 703 is thus used as write timing data with respect to the VRAM 156.

Meanwhile, the output of the ADC 126, as described above, is sent along lines 146 and lines 140 to the timing gate-array 142. Specifically, as shown in Figure 10, this data is applied to the Buffer 714 and sent along lines 722 to the FIFO circuit 702 and further to the VRAM data Buffer 701. Then, the data from the VRAM data Buffer 701 is written into the VRAM 156 along line 154 by using the write timing data generated by the VRAM address Buffer/Multiplexer 703 as described above.

Then, the computer 10 sends VGA type synchronization information by way of lines 166 and 169, as described above with respect to the first function, in order to provide VGA synchronization 703 information to the VRAM address Buffer/Multiplexer by way of the programmable sync generator 711. The programmable sync generator 711 supplies VGA synchronization data along lines 799 and 720 to the VRAM address Buffer/Multiplexer 703 and the VRAM state machine 704, respectively. Then, the VRAM state machine 704 sends a command signal along line 719 to the VRAM address Buffer/Multiplexer 703 so that the VRAM address Buffer/Multiplexer selects the synchronization information along lines 799 to be output onto line 154 to the VRAM 156 to be used as read timing data.

Thus, the data stored in the VRAM 156 is read out along lime 164, as shown in Figure 2, under a read timing dictated by the VGA synchronization format. The data read out of the VRAM 156 is sent to the switcher gate-array 168 as shown in Figure 2. More specifically, as shown in Figure 11, the data read out of the VRAM 156 is applied on line 164 to Buffer 1001 and on to the two-to-one multiplexer 1004 and on to the Buffer 1005 to the switcher gate-array 168 output line 176. At this point, the digital data is transformed to analog form by the DAC 178 and the thus-transformed data is supplied along line 180 in VGA form.

The imaging system in which the overlay and rescan board 14 interfaces the perspnal computer 10 to the rec/player 12 is successful in realizing various kinds of image processing based on the combination of a real image and VGA image. For example, as shown in FIG. 3, text data 202 may be overlaid on a screen 200 showing a real image, with digitization and/or manipulation being applied to a particular portion 204 of the screen 200. The personal computer 10 generates the text data 202 and commands the digitization or the manipulation of the text data. Digitization and manipulation include posterization, paint, shrink, and move. The processing of a real image including the overlaying of text data 202 and digitization and manipulation is effected by a sequence of steps: feeding a video signal representing a real image and inputted via the input port 102, 104 or 106 to the input 136 of the NTSC switcher 138, transferring VGA video data from the VGA RAM 174 to the VRAM 156 and reading it out of the VRAM 156 using the timing gate-array 142 which employs scan conversion and, applying the scan-converted signal to the other input 140 of the NTSC switcher 138. Then, either one of the inputs 136 and 140 is selected on a pixel-by-pixel basis, as described below, to feed the resultant signal to the output 108 through digital-to-analog converter 198. The timing gate-

arry 142 identifies the pixel timings associated with the VGA data written in the VRAM 156 and causes the NTSC switcher 138 to perform switching at those pixel timing on a pixel-by-pixel basis. Such pixel-by-pixel switching of the NTSC switcher 138 occurs under the control of the timing gate-array 142 which is responsive to the control signal 152 generated by the Gen-lock unit 150. The Gem-lock unit 150 locks the phase to the video frequency of the input 102, 104 or 106, as stated previously. The scan conversion of the VGA video data stored in the VGA RAM 174 into the NTSC format is executed by the timing gate-array 142 and video DAC 198. The video signal representing the so processed real image 200 is fed out via the NTSC output 108 and applied to the video monitar 24 or similar equipment. The pixel-by-pixel switching described above allows a real iamage and a VGA image to be mixed whithout resorting to an image data storage having a large capacity.

This is also true with the case wherein the processed real image 200 is outputted in the form of RGB type and/or S-type video signals. In this instance, the RGB switch 130, instead of the NTSC switcher 138, performs switcing on the pixel-by-pixel basis under the control of the timing gate-array 142, whereby the text data 202 and digitization and manipulation are combined with the real image 200.

In any case, the operator is capable of combining graphics and text with the real image 200 appearing on the video monitor 24 by manipulating the personal computer 10 while watching the image 200. Of course, the VGA image to be combined with the real image 200 may be of the kind giving a special effect such as scramble, wipe, scroll, offset, clip, wash, or rotate.

Now, a third function of the invention, such a function involving the overlaying of VGA video signals onto NTSC video signals will be described. Firstly, the computer 10 sends VGA information along line 192 through the bus Buffers 188 as shown in Figure 2 and on to the VGA controller 170 and further to the VGA RAM 174 along line 172. At the same time, VGA synchronization information is sent from the computer 10 along lines 166 and 169 to the timing gate-array 142. Using exactly the same operation as described above with respect to the first function, that is, transforming VGA to NTSC, the VGA data in the VGA 174 is sent through the VGA controller 170 and the switcher gate-array 168 to the VRAM 156. The data is read into the VRAM 156 using read timing data produced based on the above-mentioned VGA synchronization information supplied from the VGA controller 170 through lines 166 and lines 169 to the timing gate-array 142. Again, the VGA synchronization information is used by the timing gate-array 142 to produce write timing data with respect to the VRAM 156 in the same way as it produced the write timing data for the first function described above. Thus, the VRAM 156 now contains VGA data from the VGA RAM 174.

Meanwhile, NTSC type information is input on terminal 102 of Figure 2 and is sent to the switch 134 and further to the ADC 199 where the information is converted to digital data and then is output along line 136 to the NTSC switcher 138.

The NTSC data is also sent to the NTSC decoder 114 which transforms the NTSC data into RGB data and outputs the RGB data onto line 120. The RGB data on line 120 is next sent to RGB switch 116 where it is output onto line 124 and applied to the Gen-lock circuit 150 where, as described above, synchronization information is phase locked and sent along line 152 to the timing gate-arry 142. As shown in Figure 9 and 10, the synchronization information along line 152 is applied to the Gen-lock logic 713 of the timing gate-array 142 and the synchronization information than passes through the programmable sync generator 712 on to line 798 and is applied to the VRAM address Buffer/Multiplexer 703 and the VRAM state machine 704 in a manner as described above so that the synchronization information is output onto line 154 to be used as read timing data for the VRAM 156.

Thus, date is read out of the VRAM 156 along line 154 and supplied to the VRAM data Buffer 701. This data is in the NTSC format since the NTSC synchronization information was locked by the Gen-lock circuit 150 and sent to the timing gate-array 142. The data is next sent to the FIFO circuit 702 and is applied along lines 722 to the Buffer 714 where it is output along line 140 to the NTSC switcher 138 as shown in Figure 2.

At this point the NTSC switcher 138 receives two separate inputs. One input, as described sbove, is from the ADC 199 along line 136 and represents the NTSC information which was applied along input terminal 102. The second input, as also described above, is supplied along lime 140 from the timing gate-array 142. Inside the timing gate-array 142 the overlay logic block 716 receives a keying color, which is, for example, transparent, into an overlay color register and also receives the data being sent along lines 722 from the FIFO circuit 702 to the Buffer 714. This information passes on line 796 which connects the Buffer 714 and the Buffer 715. The data from the Buffer 714 is transferred by means of line 796 to the Buffer 715 which is in turn transferred along line 723 to the actual data register, discussed above, of the overlay block 716. Next, as fully discussed above, and as is well known in the art, the overlay logic block 716 compares the contents

of its two registers to datermine whether or not the keying color is present in the data sent from the FIFO circuit 702 a long line 722. When the keying color is present, the overlay logic block outputs on line 144, a control signal to the NTSC switcher 138 so as to cause the NTSC switcher to select the information output from the ADC 199 along line 136 to be supplied as an output of the NTSC switcher 138 and onto the DAC 198 to be finally supplied to output terminal 108.

If, in the overlay logic block 716, it is determined that keying color has not been sent from the FIFO circuit 702 along line 722, then the command signal applied along line 144 is sent to the NTSC switcher 138 so as to select the signal on line 140, which represents the information stored in the Buffer 714 of Figure 10 to be output of the NTSC switcher 138 and sent to the DAC 198 to the terminal 108.

Thus, by performing this type of pixel-by pixel-switching an overlayed image may be formed, such an overlayed image being in the NTSC format, that is, the interlaced format.

The DAC 198 also receives the control signal along line 144 from the overlay logic 716. The DAC 198, which is conventional in the art, switches to a different digital-to-analog converting scheme when the information supplied from the NTSC switcher 138 has been input on line 136 as opposed to the situation where the output of the NTSC switcher 138 is from line 140. As discussed abóve, the information originally input on line 102 and converted into digital form by the ADC 199 results in a different type of digital representation than the informaton sent from the computer 10 along line 192 to bus Buffers 188 and through the VGA controller 170 to the VGA RAM 174. The information sent by the comuputer uses a look-up table, as discussed fully above, while the information output of ADC 199 instead includes relative weights of the red, green and blue colors in its digital format. That is why the DAC 198 must be controlled, so that it can know which of the digital-to-analog conversion techniques it is to perform.

The end result on line 108 consists of an overlayed VGA type video signal onto an NTSC type video signal.

In another application, a real image may be inserted in graphics which are generated by the personal computer 10. FIG. 4 shows a specific case wherein real image is inserted in a part 212 of a VGA image 210. In FIG. 4, the VGA image 210 includes various kinds of graphics 214 generated by the personal computer 10 and stored in the VGA RAM 174 as data of a raster image. On the screen 210, for the part 212 to accommodate the real image, a color "tranparent" is designated. Alternatively, the color to be designated may be "black" or any other particular color.

Now, a fourth function of the inventive overlay and rescan board will be described, such a function being an overlay operation in which NTSC information is overlayed onto VGA information. First, a brief description of this operation will be presented, and immediately following, a detailed description of this function will be laid out.

More specifically, to overlay on the screen of the VGA monitor 16 the digitized video data stored in the VRAM 156 and the VGA graphics and text data stored in the VGA RAM 174, use is made of the mode indication bit #15 of the video data word. Generally, digitized video data and graphics and text data are represented in the true-color mode and the pseudo-color mode, respectively. The switcher gate-array 168 switches the two types of video data, while the video DAC 178 converts them into corresponding analog outputs. The true-color mode video data are converted into analog signals without a look up table being used, but the pseudo-color mode video data cannot be converted into color signals if a look-up table is not used. The switcher gate-array 168 references the mode bit #15 shown in FIG. 5 for each of the pixel data associated with the VGA video data and real image video data read out of the VGA RAM 174 and VRAM 156, respectively, and it instructs the video DAC 178 whether or not a look up table for conversion is needed. The switcher gate-array 168 identifies the pixel timings at which the color "transparent" of the VGA data has been designated and performs switching such that the real image data from the VRAM 156 are fetched at those timings on a pixel-by-pixel basis. The video data with the real image being inserted in the area of the VGA image 210 by the above procedure are converted into an analog VGA signal by the video DAC 178 and then fed out to the VGA monitor 16 via the output 180. The operator, therefore, can set the real image in the VGA image 210 appearing on the VGA monitor 16 by operating the personal computer 10 while watching the monitor 16. If desired, various special effects may be incorporated by the manipulation of the personal computer 10.

Now, a detailed description of the fourth function will be described. VGA information is sent from the personal comuputer 10 along the line 192 through the bus Buffers 188 through the VGA controller 170 along line 172 to the VGA RAM 174.

Meanwhile, NTSC information is input at terminal 102 and applied to the NTSC decoder 114 which transforms the NTSC information to RGB information and sends the RGB information along lime 120 to the RGB switch 116 whose output on

line 124 goes to the ADC 126 and the Gen-lock circuit 150. The Gen-lock circuit is a phase lock loop which locks the phase of the RGB signal and sends the locked phase to the timing gate-array 142. The output of the ADC 126 is sent to the timing gate-array 142 along lines 146 and 140.

The Gen-lock logic circuit 713 receives the locked phase of the NTSC signal sent along line 152 and sends this locked phase to the programmable sync generator 712 which supplies the synchronization information along line 798 to the VRAM address Buffer/Multiplexer 703 and along line 706 to the VRAM state machine 704. As described above, the VRAM state machine 704, as a result of receiving the synchronization information along line 706, sends a control signal along line 719 to the VRAM address Buffer/Multiplexer 703 so as to cause the VRAM address Buffer/Multiplexer 703 to output on line 154 the NTSC synchronization information provided along line 798. The synchronization information along line 154 is supplied to the VRAM 156 as write timing data.

The output of the ADC 126 in Figure 2 is sent to the timing gate-array 142 and specifically enters the Buffers 714 where the data is sent along line 722 to the FIFO circuit 702 and onto the VRAM data Buffer 701 where the data is held until it is controlled by the write timing data output from the VRAM address Buffer/Multiplexer 703. The data is then written to the VRAM 156 under control of the write timing information along line 154.

Then, the VGA data is outputted from the VGA RAM 174 by means of the VGA controller along line 172 and the information is sent through the information controller 170 to the switcher gate-array 168 along line 166.

Specifically, as shown in Figure 11, the information from the VGA controller 170 enters the switcher gate-array 168 along line 166 and is applied to the Buffer 1002 where it is supplied to the two-to-one multiplexer 1004. The VGA data output from the VGA controller 170 is also applied along lines 166 and 169 to the timing gate-array 142. Specifically, the synchronization information along line 169 is applied to the programmable sync generator 711 and sent along line 799 to the VRAM address Buffer/Multiplexer 703 and along line 720 to the VRAM state machine 704. The VRAM state machine 704 sends a control signal along line 719 to the VRAM address Buffer/Multiplexer 703 which selects the VGA synchronization information from line 799 as the signal to be applied to the output of the VRAM adress Buffer/Multiplexer 154 as read control data. Information is thus read out of the VRAM 156 using the read control data along line 154 using the VGA synchronization information and the read out data is sent along line 164 as shown in Figure 2 and applied to the Buffer 1001 as shown in Figure 11 of the switcher gate-array 168. The information stored in the Buffer 1001 of Figure 11 is next sent to the two-to-one multiplexer 1004.

Looking back at Figure 10, the overlay logic block 716 receives the VGA data that is sent along lines 166 and 169, as described above to the timing gate-array 142 and, specifically, the data is sent to Buffer 715 and through lime 723 is applied to the overlay logic block 716. In this way, the VGA information may be monitored by the overlay logic block 716 in order to detect when the VGA data contains the keying color described above. This color can be, for example, transparent. When the overlay logic block 716 detects that the keying color is included in the VGA data sent to the logic block 716 through Buffer 715 and line 723, a control signal is sent along line 144 to a control input of the two-to-one multiplexer 1004 as shown in Figure 11. The control signal along line 144 thus selects the signal from Buffer 1001 to be sent as an output of the multiplexer 1004 and which is further sent to the Buffer 1005 and applied as an output 176 of the switcher gate-array 168.

When the keying color has not been datected by the overlay logic block 716 of Figure 10, a control signal is sent along line 144 to the control input of the two-to-one multiplexer 1004 so as to select the signal stored in the Buffer 1002 to be applied as an output of the multiplexer 1004 and sent to the Buffer 1005 to an output 176 of the switcher gate-array 168. Thus, pixel-by-pixel switching may be performed with respect to the data in Buffer 1001, which was originally input into terminal 102 and the data stored in Buffer 1002 which was originally input by means of the computer 10 of Figure 1.

The output of the switcher gate-array 176 is sent to DAC 178 where the information is converted into analog form to be supplied as an overlayed NTSC onto VGA signal at terminal 180. The DAC 178 performs two types of digital-to-analog conversion and the contorol signal 144 is also sent as a control input to the DAC 178 to tell DAC which type of digital-to-analog conversion to follow, in an analogous manner as the DAC 198, as described above.

Thus, as fully described above with respect to the four functions of operation of the inventive overlay and rescan board 14, a variety of video processing functions using a variety of types of video signals can be accomplished using the minimum amount of hardware.

In an imaging system wherein the overlay and rescan board 14 interfaces the personal computer 10 to the rec/player 12, various kinds of image processing are available on the basis of the combination of a real image and a VGA image. In the illustrative embodiment, a group of images can be

simply compressed into a composite image. This mechanism is useful for summarizing the contents of many images, i.e. generating a table of contents, in a compact and useful fashion. For example, as shown in Fig. 13, a plurality of reduced images 252 may be arranged in a single video frame 250 to constitute a single index image as a whole. While applicable for any reduction factor n, the case for n = 5 works as follows. With a factor of 5 reduction, 25 normal size pictures 252 can be compressed into a single image 250. The compression is implemented by simply storing only every 5th pixel/line of the image. As a result, 25 images are compressed into a single composite image 250. For reduction factors in the range of 2 to 7, the content of the original image is still easily recoguizable. This feature is implemented by the inventors in a software program for the case of n = 5. Although it is well known to simply reduce images in size using a suitable reduction factor, it is not well-known to take the reduced images and form an index image.

A video signal representative of a real image stored in the video floppy 18 is read out by the rec/player 12 and applied to the input port 102, 104 or 106 depending on whether the video signal is NTSC, RGB or S-video, respectively. The reduction of a real image and the generation and recording of the index image 250 is executed by writing the video signal applied to the input port 102, 104 or 106 and representing one video frame and real image 250 to the VRAM 156 through the timing gate array 142, and then reading out the video data skippingly at intervals determined by a given reduction ratio while writing them to the VGA RAM 174. The computer 10 sends read address information to the CPU counter 705 in Fig. 9 along line 192. In this way, address data enabling the above-described reduction ratio may be applied to the VRAM 156 by means of the VRAM address Buffer/Multiplexer 703. Line 21 leads this information to the VRAM state machine 704 which sends a command signal 719 to the Buffer/Multiplexer 703 so as to select the output of the CPU counter 705 as the Buffer/Multiplexer output on line 154.

As a result, data representative of reduced images 252 are formed in the VGA RAM 174. In the VGA RAM 174, video data representative of a reduced image 252 is written in a particular location of a bit map where the reduced image 252 is to be formed. In this manner, the illustrative embodiment allows video data representative of twenty-five video frames of reduced images 252 to be written to the VGA RAM 174, completing one frame of index image 250. To form an index image by skipping pixel data as mentioned above, the personal computer 10 controls the timing gate-array 142, as described above with respect to the CPU counter 705, and the switcher gate-array 168, by sending an enable signal to the control logic 1007 to enable buffer 1003 of Fig. 11 via bus 192.

As the video data representing the index image 250 is completed in the VGA RAM 174, it is read out and temporarily stored in VRAM 156. The video data stored in the VRAM 156 is read out by the timing gate-array 142 in the following fashion.

The programmable sync generator 712 experiences its free-running mode since no RGB signal is being applied to the Gen-lock circuit 150 in Fig. 2. Thus, the computer 10 sends, for example, NTSC type sync signals to the generator 712 along line 717 in Fig. 11. The sync signals are then sent as address control signals for the VRAM 156 by means of the VRAM address Buffer/Multiplexer 703, the VRAM state machine 704 and lines 798, 706 and 154. The data in VRAM 156 is then read out and sent through VRAM data buffer 701, FIFO circuit 702, line 772, and buffer 714 to line 140. From there, the data is sent to the NTSC switcher 138. The resulting video signal representative of the index image 250 is delivered from the NTSC output 108 to be used by the video monitor 24 or similar equipment.

Further, a characteristic feature of the illustrative embodiment is that the video signal representing the index image 250 is written to the video floppy disk 18 by the rec/player 12. The video floppy 18 stores video signals representative of the original images with which the reduced images 252 included in the index image 250 are associated. The video signal representative of the index image 250 is written to a particular track of the floppy 18 by the rec/player 12. The user of the rec/player 12 may reproduce the index image 250 stored in the particular track, i.e., index track later so as to see the contents of the floppy 18 in a summarized fashion.

In an application, as shown in Fig. 14 the illustrative embodiment allows a title or similar text or graphics 260 to be combined with the index image 250. Such processing of the index image 250 inducing the insertion of the text and/or graphics 260 is implemented by manipulating the video data stored in the VGA RAM 174 on the personal computer 10. Specifically, the user operates the personal computer 10 to generate a text or graphics such as "Fuji" as shown in Fig. 12 and marks a desired area of the index image 250 for inserting the text or graphics 260. These data are fed from the personal computer 10 to the overlay and rescan board 14 via the bus 192 to be written to the designated area of the bit map data of the VGA RAM 174. Consequently, video data representative of the index image 250 including that title 260 are completed in the VGA RAM 174. These data are read out of the VGA RAM 174 by the previously

stated sequence and temporarily stored in the VRAM 156. Thereafter, the video data are read out of the VRAM by the previously described operation and applied to NTSC output teminal 108, where the titled index image may be either displayed on an NTSC monitor or written to a floppy disc. Of course, the video data may also be fed from the VGA RAM 174 to the video DAC 178 via the switching gate-array 168 and thereby be also reproduced on the VGA monitor 16 as a VGA type video signal.

In addition, with the illustrative embodiment, it is possible to combine a title or similar text and/or graphics with one video frame of a real image represented by video data which is read out of the video floppy 18. Specifically, a video signal representing a real image and stored in the video floppy 18 is read out by the rec/player 12 and then written to the VRAM 156 via the input port 102, 104 or 106. During this write operation, the Gen-lock circuit 150 of Fig. 2 outputs sync information to the Gen-lock logic block 713 of Fig. 10 and also to the programmable sync generator 712. The sync information is further provided, on lines 798 and 706 to the VRAM address Buffer/Multiplexer 703 and the VRAM state machine 704 where address write timing information is formed based on the sync information. The video signal is read out of the VRAM 156 on line 164 and fed to the VGA RAM 174 via the switcher gate-array 168. During this read-out, computer 10 sends a command signal on line 192 to the control logic 1007 of Fig. 11 so as to enable the buffer 1003. The text or graphics 260 generated by the personal computer 10 are written to a desired area of the bit map of the real image which is represented by the video data stored in the VGA RAM 174.

While the index image 250 is formed in the VGA RAM 174 as a bit map, it is displayed on the VGA monitor 16 by sending the data through the VGA contoroller 170 and to the switcher gate array 168 and finally through the DAC 178 to output terminal 180 so as to facilitate the operator's manipulation. During this time period the computer 10 disables the Buffer 1003 by means of control logic 1007. The bit map data stored in the VGA RAM 174 is read out and fed to the switcher gate-array 168 under the control of a VGA controller. The switcher gate-array 168 delivers the VGA video data to the video DAC 178 which then converts it into acorresponding VGA type analog video signal. By such a procedure, the index image 250 stored in the VGA RAM 174 is applied as a VGA video signal to the VGA monitor 16 to be displayed thereon. Of course, the video data representative of the index image 250 may be fed to and displayed on the NTSC monitor 24, in which case the video data will be once fed to the NTSC switcher 138 via the VRAM 156 and therefrom to the NTSC monitor 24 via the rec/player 12. During this operation the computer 10 has enabled the Buffer 1003 by means of control logic 1007. This is also true with the case wherein the index image 250 is outputted in the form of an RGB type and/or S-type video signal. In such a case, the video signal will be routed through RGB switch 130 in place of the NTSC switcher 138. In any case, the operator manipulates the personal computer 10 to insert graphics and text in the index image 250 appearing on the video monitor 24 or the VGA monitor 16 while watching it, whereby the title 260, for example, may be combined with the index image 250.

The rec/player 12 may be implemented as a video data recording and reproducing apparatus capable of recording and playing back a video tape. In such an application, the system may summarize the scenes recorded in a video tape and write the summary to the video tape. This summary is produced by reading video signals out of the video tape by the rec/player 12, writing them to the VRAM 156, and then editing them by use of the VGA RAM 174, in the same manner as with the index image of still pictures stored in the video floppy. A title or similar text and graphics may also be inserted in the same manner with the index image of still pictures.

FIG. 15 shows a modification of the overlay and rescan board of Fig. 2, and only the modified parts are shown. The modification allows overlaid NTSC-type video signals onto VGA-type signals to be displayed on not only a VGA monitor as described above, but also on an NTSC-type monitor as well. A line 1103 is tapped off the switcher gate array 168 output 176 which contains an overlaid NTSC type video signal onto a VGA-type signal. The overlaid signal is fed through line 1103 to a line buffer 1101 which stores one line of image data at a time. Lines of data corresponding to the overlaid signal are successively written into the line buffer 1101 at a frequency of, for example, 31.500 KHz, which is the frequency at which one line of VGA-type image data is applied to a monitor during the formation of a VGA image.

Lines of data are successively read out of the line buffer 1101 at a frequency of exactly one-half the frequency at which the lines were written into the line buffer. Thus, the read out frequency is 15.750 KHz, which corresponds to the frequency at which one line of NTSC-type image data is applied to a monitor during the formation of an NTSC-type image. Thus, the line buffer 1101 acts as a scan-converter, such as the one shown in Fig. 6.

NTSC-type video lines are interlaced, meaning that first, for example, all even numbered lines are displayed and then all odd-numbered lines are displayed interwoven amongst the already-dis-

played even-numbered lines. Thus, the line buffer 1101 output at first, for example, corresponds to even numbered scan lines and, after all of the even numbered scan lines have been displayed, the computer 10 sends a timing control signal along line 1102 to produce a phase-shift of one line in the line buffer read out process, so that the odd-numbered lines are next read out. In this way, the interlaced NTSC-type format can be created from a non-interlaced VGA-type format input. Thus, an overlaid NTSC-type video signal onto a VGA-type signal in a VGA-type format (i.e., non-interlaced) by be transformed into an overlaid signal in an NTSC-type format (i.e., interlaced). As a result, overlaid images may be provided to both a VGA-type monitor and an NTSC-type monitor.

Another embodiment of the invention will now be described in which storage of a composite overlaid signal is made possible. As described above, the rate at which the overlaid signals are output on terminals 108, 110, 112 or 180 is too high to enable an external memory device to receive the overlaid signals. Therefore, a modification to the overlay and rescan board of Fig. 2 has been designed by the inventors and is shown in Fig. 16. For the sake of simplicity, only the circuit elements of Fig. 2 needed to show the modification are shown in Fig. 16. Also, for the sake of simplicity, only the electrical connections which have been added to Fig. 2 in order to create the modification are shown in Fig. 16.

As is clear from Fig. 16, feedback connections have been added to the circuit of Fig. 2 in order to send overlaid signals back to the frame memories. More specifically, feedback line 991 is connected from the output of NTSC switcher 138 back to the input of VGA controller 170, so that an overlaid VGA onto NTSC signal may be stored into VGA RAM 174 under the control of VGA controller 170. Likewise, feedback line 992 is connected from the output of RGB switch 130 back to the input of VGA controller 170, so that an overlaid VGA onto RGB or S-type video signal may be stored into VGA RAM 174 under the control of VGA controller 170.

Feedback line 993 is provided from the output of switcher gate array 168 back to the input of timing gate array 142 so that overlaid NTSC, RGB, or S-type video signals onto VGA image signals may be stored into VRAM 156 under the control of timing gate array 142.

The above-described feedback paths are merely exemplary. Any of the switcher 138, 130 or 168 outputs may be fed back to any of the controller 142 or 170 inputs to temporarily store the overlaid images. Further, not only overlaid images but also output signals representing images that have been converted from one image format, i.e., VGA, to another, i.e., NTSC, may be fed back and stored in memories 156 or 174.

In order to enable output signals to be fed back to either the timing gate array 142 or the VGA controller 170 the personal computer 10 sends commands through bus buffers 188 to these circuit elements to stop receiving new image data through ADC 126 and from the computer 10 respectively. Then, the circuit elements 142 and 170 are switched to a write mode where they cause overlaid images from the outputs of circuit elements 138, 130 or 168 to be written into memories 156 or 174.

With respect to the feeding back by means of line 993 of signals from the switcher gate array 168 output 176, the signal passes on line 993 to the Buffer 715 of the timing gate array 142 as shown in Fig. 10. Programmable sync generator 711 receives VGA timing data from a Gen-lock circuit (not shown) so as to send the timing data along line 799 and line 720 to the VRAM address Buffer/Multiplexer 703 and the VRAM state machine 704, respectively. The VRAM Buffer/Multiplexer 703 is thus instructed by the VRAM state machine 704 to choose its input line 799 to be output onto its output line 154 where it is supplied to VRAM 156 as write thing data.

Meanwhile, the VGA format data which was sent along line 993 of Fig. 16 to Buffer 715 of Fig. 10 is sent, by means of lines 796 and 722 to the FIFO circuit 702 and the VRAM Data Buffer 701. From there the data is written into VRAM 156 under the control of the write timing data supplied from the VRAM address Buffer/Multiplexer 703, as described above.

By feeding the overlaid images back into the VRAM 156 or the VGA RAM 174 and storing them in the VRAM 156 or the VGA RAM 174, the thus-stored overlaid images may be then transferred from the internal memories 156 or 174 to an external memory at a transfer rate which the external memory can handle. Thus, the overlaid images stored in external memory devices may be easily and selectably read out and displayed on a monitor at a later time without having to re-overlay the image signals making up the composite overlaid signal. Also further processing or overlaying of the overlaid signals is greatly simplified.

While the present invention has been described with reference to the particular illustrative embodiments, it is not to be restricted by those embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change or modify the embodiments without departing from the scope and spirit of the present invention.

BNSDOCID: <EP 0484981A2>

Claims

1. An image data processing apparatus for processing image data representative of real image or graphics image,
CHARACTERIZED IN THAT
said apparatus comprises:
randomly accessible first storing means (156) for rewritably storing image data representative of one image frame;
first inputting means (188) connected to a bus (192) of a processing system (10) for inputting a first type of image data to said first storing means, said first type of image data being formatted to be compatible with said processing system;
first control means (142) for controlling write-in and read-out of image data with respect to said first storing means;
second inputting means (102, 104, 106, 114, 118, 126, 142, 150,) for inputting a second type of image data representative of a real image and inputting said second type of image data to said first control means;
first outputting means (168, 178, 180) connected to said first control means for outputting image data of said first type; and
second outputting means (130, 138, 191, 198, 158, 108, 110, 112) connected to said first control means for outputting image data of said second type; wherein
said first control means includes selective storing means (711, 712) for selectively storing image data input to said apparatus by either said first or said second inputting means into said first storing means based on commands from said processing system; and
said first control means also includes selective reading means (711, 712, 714, 715) for selectively reading out image data stored in said first storing means as either image data of said first or said second type based on commands from said processing system, and feeding said first and said second type of image data to said first and said second outputting means, respectively.

2. An apparatus according to claim 1
CHARACTERIZED IN THAT said apparatus further includes conversion means (1001) located between said first outputting means and said second outputting means for converting a signal of said first type applied to said first outputting means to a signal of said second type and for supplying the thus converted signal to said second outputting means.

3. An image data processing apparatus or processing image data representative of real image or graphics image,
CHARACTERIZED IN THAT
said apparatus comprises:
randomly accessible first storing means (156) for rewritably storing image data representative of one image frame;
first inputting means (188) connected to a bus (192) of a processing system for inputting a first type of image data to said first storing means, said first type of image data being formatted to be compatible with said processing system;
first control means (142) for controlling write-in and read-out of image data with respect to said first storing means;
second inputting means (102, 104, 106, 114, 118, 116, 126, 150) for inputting a second type of image data representative of a real image and inputting said second type of image data to said first control means;
first outputting means (168, 178, 180) connected to said first control means for outputting image data of said first type; and
second outputting means (130, 138, 191, 198, 158, 108, 110, 112) connected to said first control means for outputting image data of said second type; wherein
said first control means includes selective storing means (711, 712) for selectively storing image data input to said apparatus by either said first or said second inputting means or image data appearing at either said first or said second into said first storing means based on commands from said processing system; and
said first control means also includes selective reading means for selectively reading out image data stored in said first storing means as either image data of said first or said second type based on commands from said processing system, and feeding said first and said second type of image data to said first and said second outputting means, respectively.

4. An apparatus according to claim 1, 2 or 3
CHARACTERIZED IN THAT the image data is stored in said first storing means in the form of digital data.

5. An apparatus according to claim 4
CHARACTERIZED IN THAT the image data stored in said first storing means includes a first indication indicating whether the stored image data was input to said apparatus by said first or said second inputting means; and
said first outputting means comprising first

signal converting means (178) for converting, upon receiving image data of said first type, the received image data of said first type into an analog image signal of one of two formats depending upon said first indication.

6. An apparatus according to claim 5 CHARACTERIZED IN THAT said first inputting means comprises:

second storing means (174) connected to the bus of the processing system for storing said first type of image data received over said bus; and

second control means (170) for reading said first type of image data out of said second storing means to write said first type of image data to said first storing means.

7. An apparatus according to claim 6 CHARACTERIZED IN THAT said first image data input to said apparatus through said first inputting means has a data format including a second indication indicative of an address of a look-up table which designates a color for forming pixels.

8. An apparatus according to claim 7 CHARACTERIZED IN THAT said first outputting means further comprises first switch means (1004) for outputting image signals, which were input to said apparatus through said second inputting means and which are stored in said first storing means, when said second indication of image signals stored in said second storing means designates a predetermined color and for outputting image signals stored in said second storing means otherwise.

9. An apparatus according to claim 8 CHARACTERIZED IN THAT said predetermined color is transparent.

10. An apparatus according to claim 9 CHARACTERIZED IN THAT said second outputting means comprises:

second signal converting means (191, 198) for converting, upon receiving image data of said second type, the received image data of said second type into an analog signal of one of two formats depending upon said first indication; and

second switching means (130, 138) for receiving image signals which were input through said second inputting means and which were sent directly to said second switching means as a primary second switching means input signal and image signals which were input to said apparatus through said first inputting means and which were stored in said first storing means as a secondary second switching means input signal, and for outputting said primary second switching means input signal when said second indication of said secondary second switching means input signal designates a predetermined color and for outputting said secondary second switching means input signal otherwise;

said first control means reading, in synchronism with said primary second switching means input signal, said secondary second switching means input signal out of said first storing means to feed said secondary second switching means input signal to said second outputting means and causing said second switching means to switch on a pixel-by-pixel basis, whereby said primary second switching means input signal is combined with said secondary second switching means input signal.

11. An apparatus according to claim 1, 2 or 3 CHARACTERIZED IN THAT image data input to said apparatus through said second inputting means comprises a television signal.

12. An apparatus according to claim 2 CHARACTERIZED IN THAT said conversion means comprises a line buffer.

13. An apparatus according to claim 12 CHARACTERIZED IN THAT said line buffer is capable of being written to at one frequency and being read from at another frequency so as to perform scan conversion.

14. A memory system for use in an image data processing apparatus,

CHARACTERIZED IN THAT

said memory system comprises:

an image data memory (156); and

programmable control means (142) for reading and writing image data to and from said image data memory using a variety of read/write timing data formats so that a variety of image data formats may be written to and read from said image data memory.

15. A memory system according to claim 14 CHARACTERRIZED IN THAT image data to be written to said image data memory is first input to said control means, and said control means receives timing data corresponding to the received image data so as to program said control means to write the received image data to said image data memory using write timing data corresponding to the received timing data.

16. A memory system according to claim 14 CHARACTERIZED IN THAT image data to be written to said memory is sent directly to said memory, and timing data corresponding to the image to be written to said memory is sent to said control means so as to program said control means to write the image data to said memory using write timing data corresponding to the received timing data.

17. A memory system for use in an image data processing apparatus,
CHARACTERIZED IN THAT
said memory system includes:
an image data memory(156); and
a programmable control system for reading and writing image data to and from said image data memory using a variety of read/write timing data formats so that a variety of image data formats may be written to and read from said image data memory.

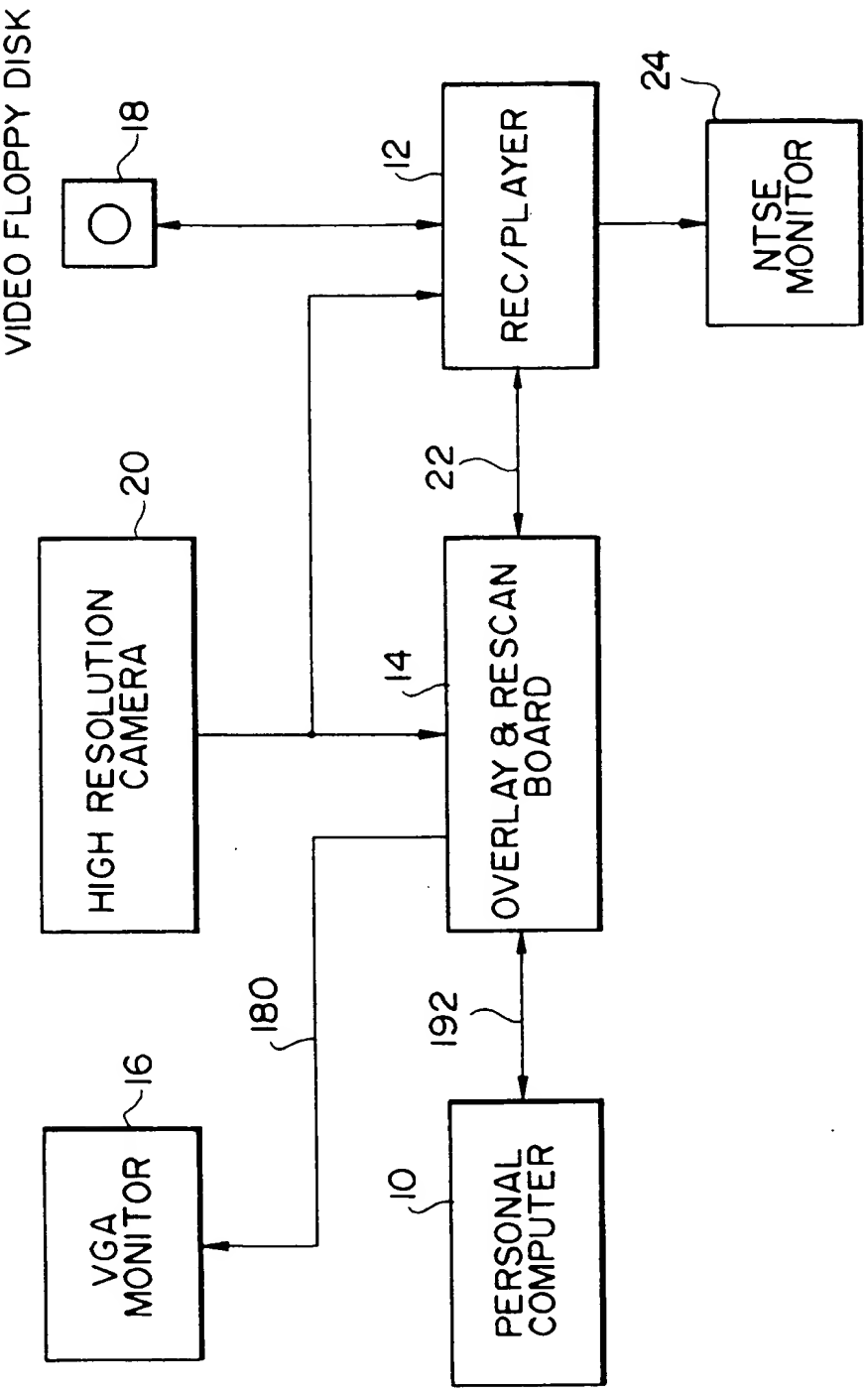
VIDEO FLOPPY DISK
18
12
REC/PLAYER
24
NTSE MONITOR
20
22
HIGH RESOLUTION CAMERA
14
OVERLAY & RESCAN BOARD
180
192
16
VGA MONITOR
10
PERSONAL COMPUTER

FIG.1

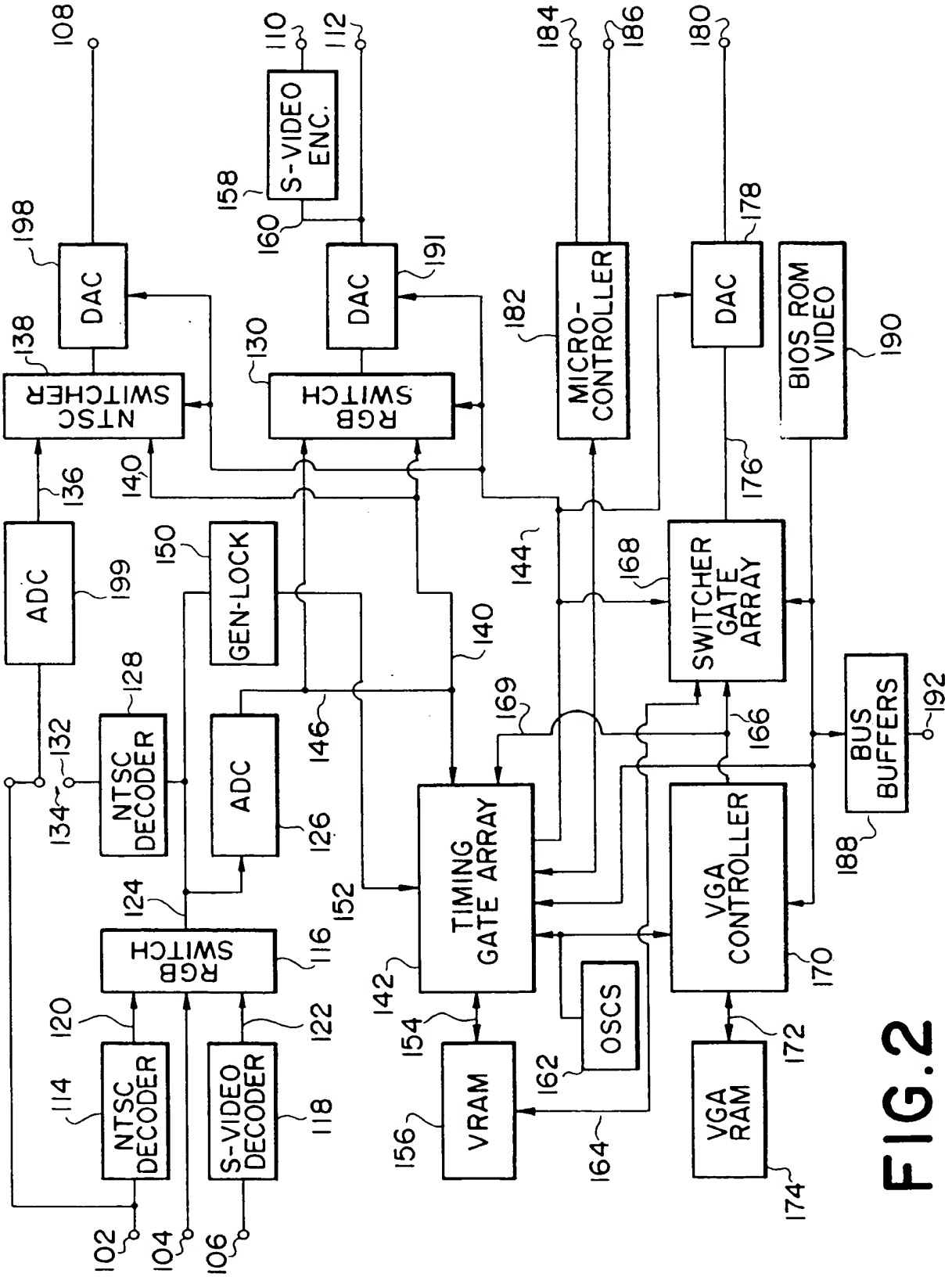
108
110
112
184
186
180
158
S-VIDEO ENC.
160
198
DAC
191
DAC
182
MICRO-CONTROLLER
DAC
178
BIOS ROM VIDEO
190
138
NTSC SWITCHER
130
RGB SWITCH
136
140
176
ADC
199
150
GEN-LOCK
144
168
SWITCHER GATE ARRAY
128
132
NTSC DECODER
ADC
146
140
169
166
BUS BUFFERS
192
134
126
124
152
TIMING GATE ARRAY
RGB SWITCH
116
VGA CONTROLLER
188
120
122
142
154
OSCS
170
114
NTSC DECODER
S-VIDEO DECODER
118
162
172
156
VRAM
164
VGA RAM
174
102
104
106

FIG.2

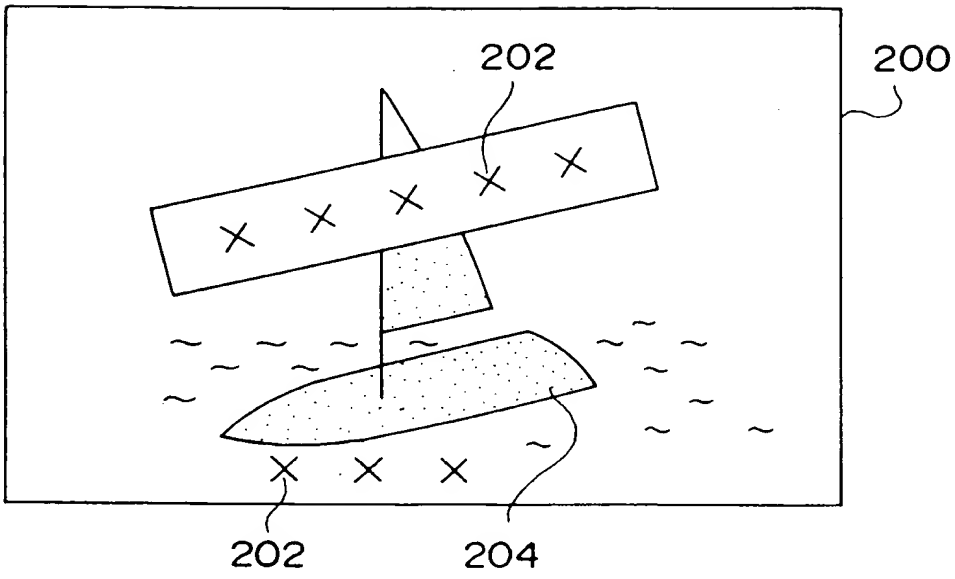

FIG.3

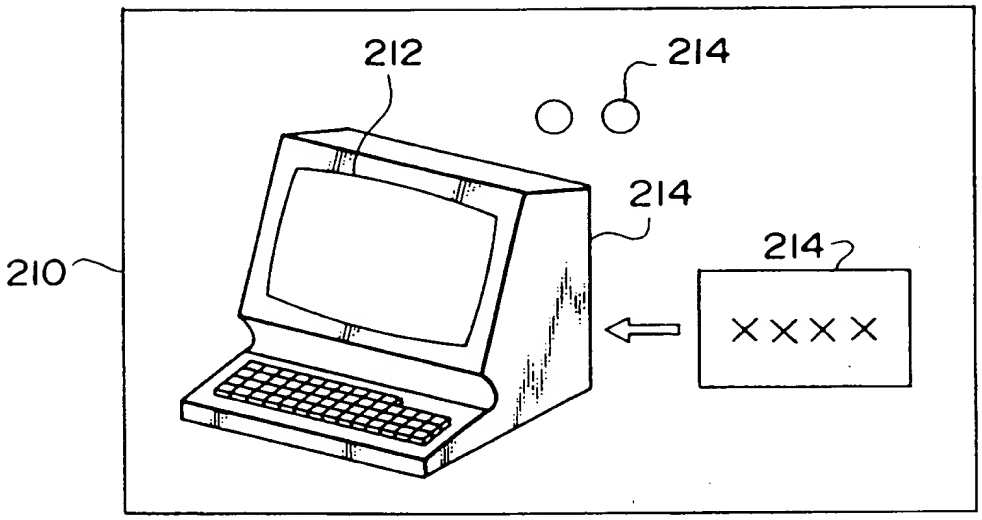
212
214
214
214
210
XXXX

FIG.4

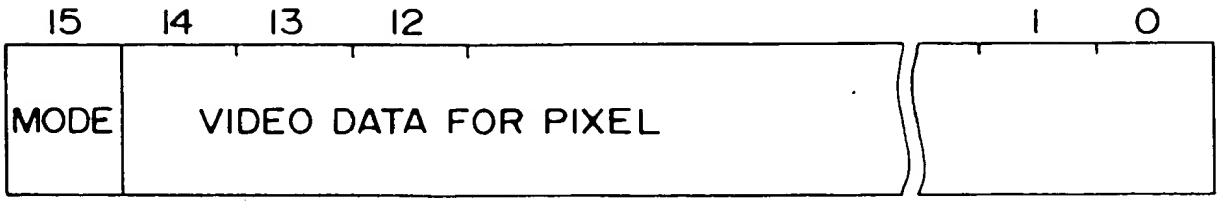
15
14
13
12
1
0
MODE
VIDEO DATA FOR PIXEL

FIG.5

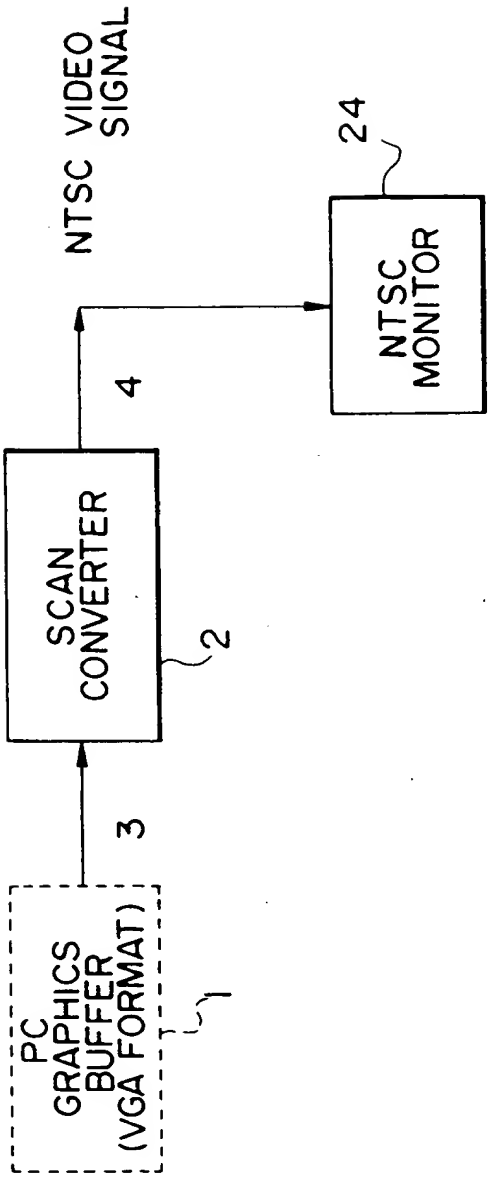
PC GRAPHICS BUFFER (VGA FORMAT)
1
3
SCAN CONVERTER
2
4
NTSC VIDEO SIGNAL
24
NTSC MONITOR

FIG.6

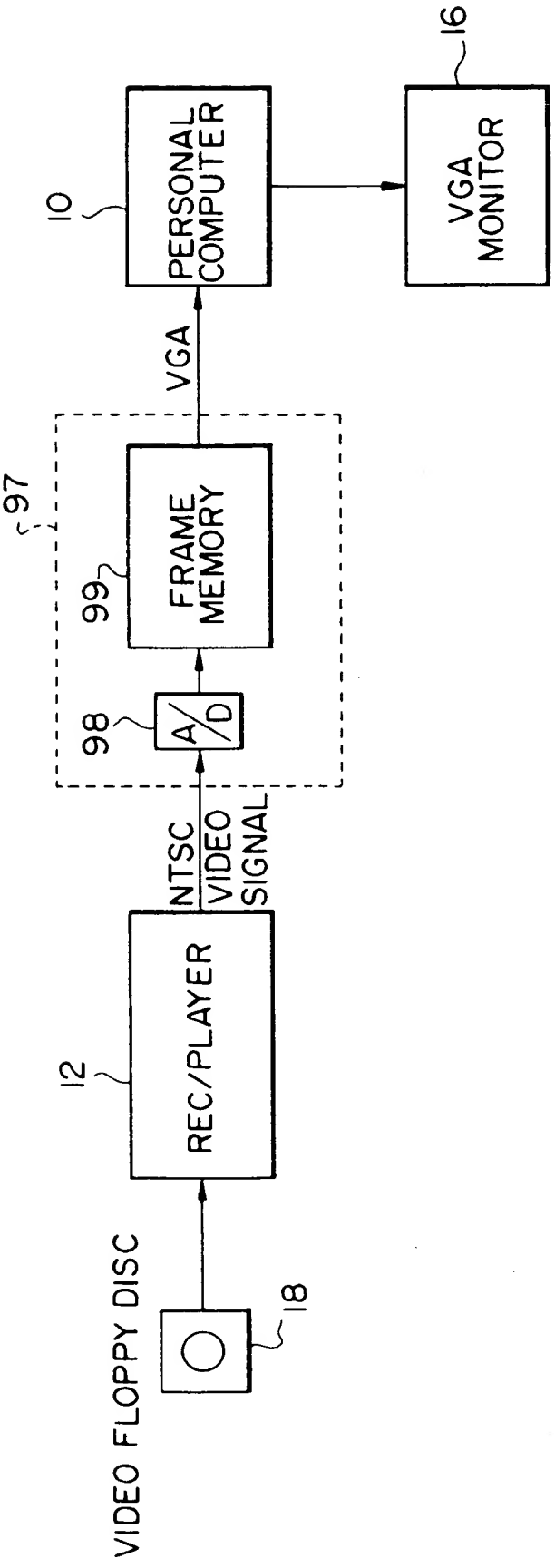
VIDEO FLOPPY DISC
18
12
REC/PLAYER
NTSC VIDEO SIGNAL
97
98
A/D
99
FRAME MEMORY
VGA
10
PERSONAL COMPUTER
16
VGA MONITOR

FIG.7

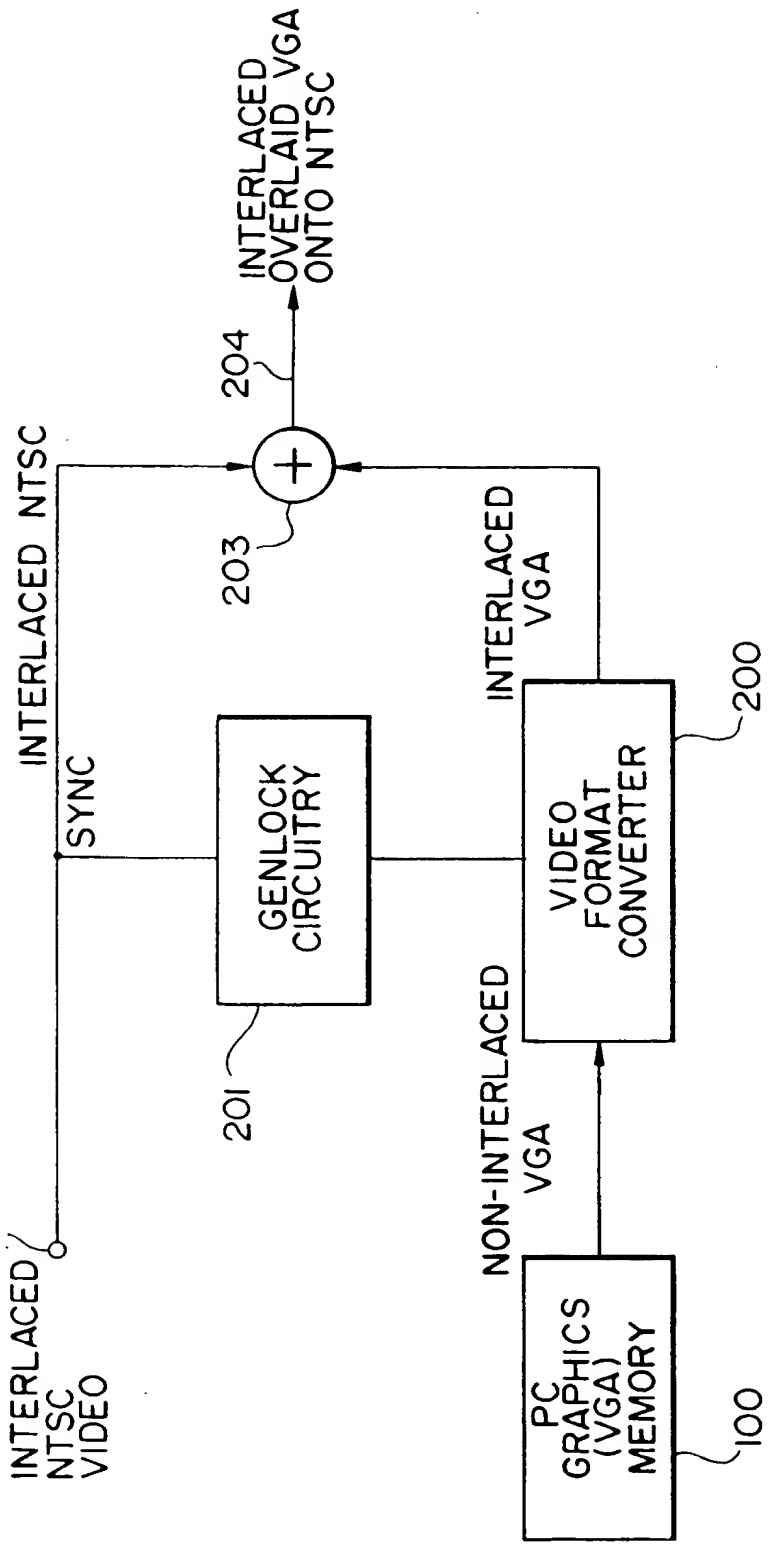
INTERLACED OVERLAID VGA ONTO NTSC
204
INTERLACED NTSC
203
INTERLACED VGA
SYNC
GENLOCK CIRCUITRY
VIDEO FORMAT CONVERTER
200
201
NON-INTERLACED VGA
202
INTERLACED NTSC VIDEO
PC GRAPHICS (VGA) MEMORY
100

FIG.8

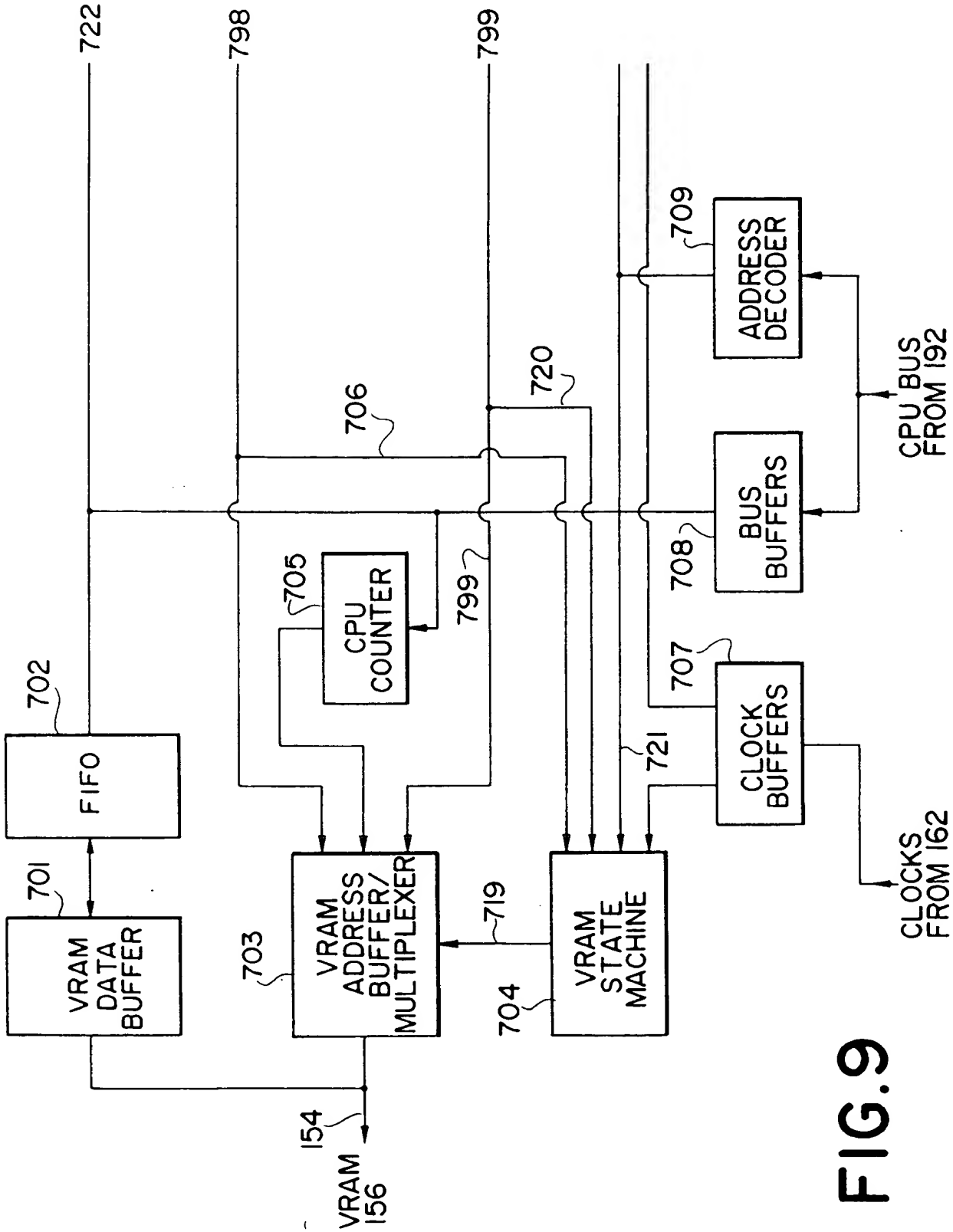
722
798
799
709
ADDRESS DECODER
CPU BUS FROM 192
720
706
BUS BUFFERS
708
705
CPU COUNTER
799
707
CLOCK BUFFERS
721
CLOCKS FROM 162
702
FIFO
701
VRAM DATA BUFFER
703
VRAM ADDRESS BUFFER/ MULTIPLEXER
719
704
VRAM STATE MACHINE
154
VRAM 156

FIG.9

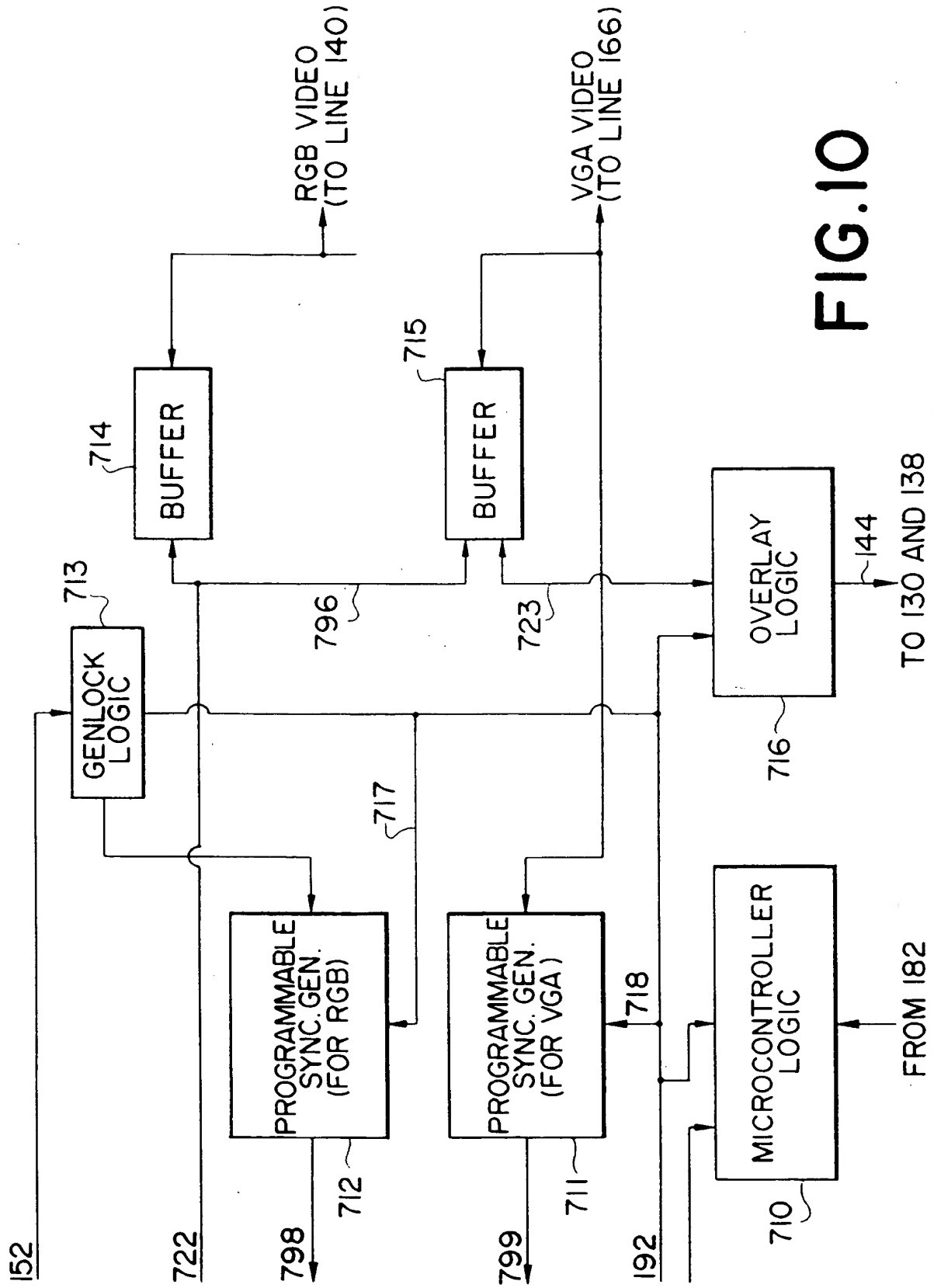
RGB VIDEO (TO LINE 140)
VGA VIDEO (TO LINE 166)
BUFFER
714
BUFFER
715
GENLOCK LOGIC
713
796
723
OVERLAY LOGIC
144
TO 130 AND 138
716
717
PROGRAMMABLE SYNC. GEN. (FOR RGB)
712
PROGRAMMABLE SYNC. GEN. (FOR VGA)
711
718
MICROCONTROLLER LOGIC
710
FROM 182
152
722
798
799
192

FIG.10

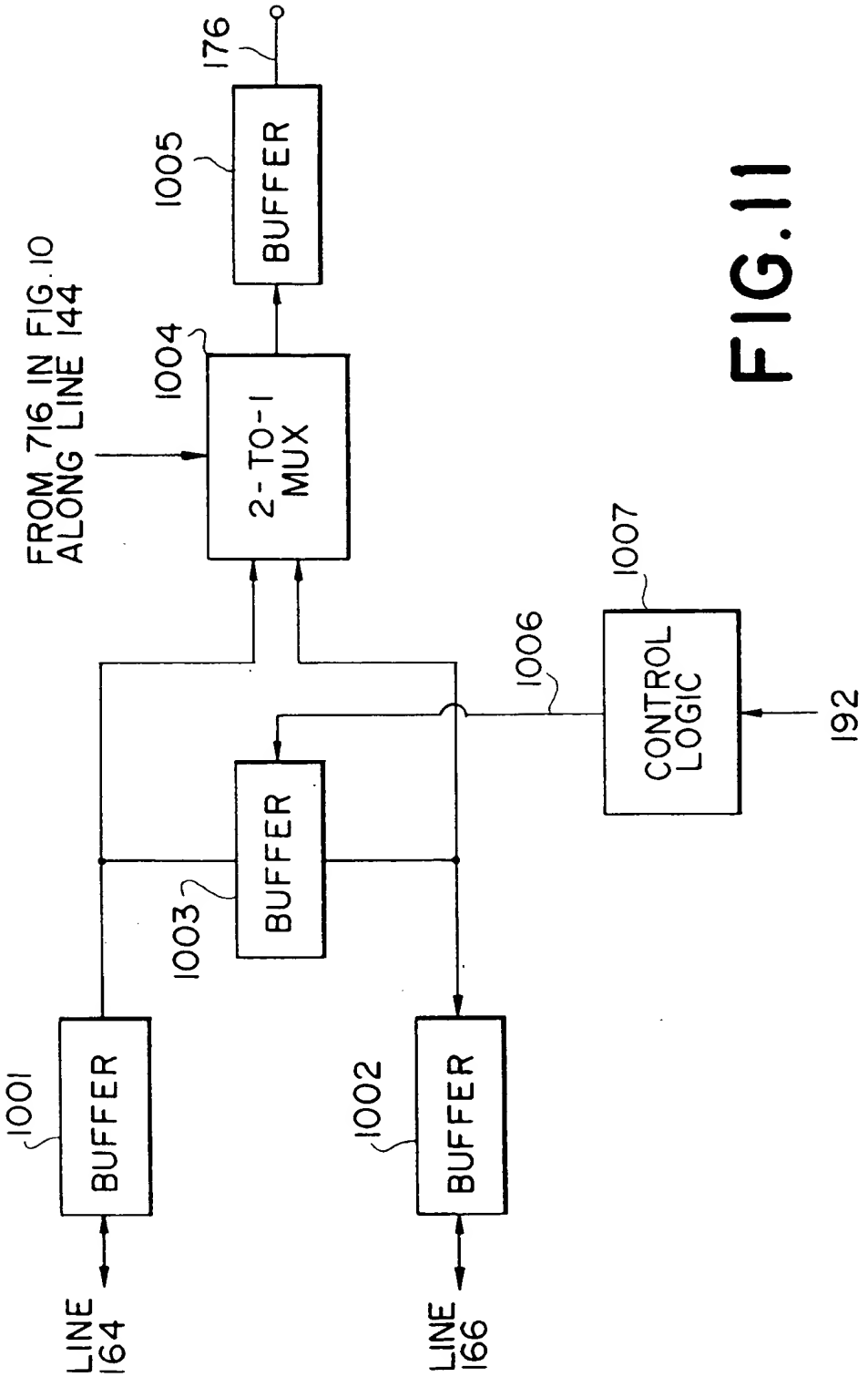
FROM 716 IN FIG. 10 ALONG LINE 144
2-TO-1 MUX
1004
BUFFER
1005
176
BUFFER
1003
BUFFER
1001
BUFFER
1002
CONTROL LOGIC
1006
1007
192
LINE 164
LINE 166

FIG. 11

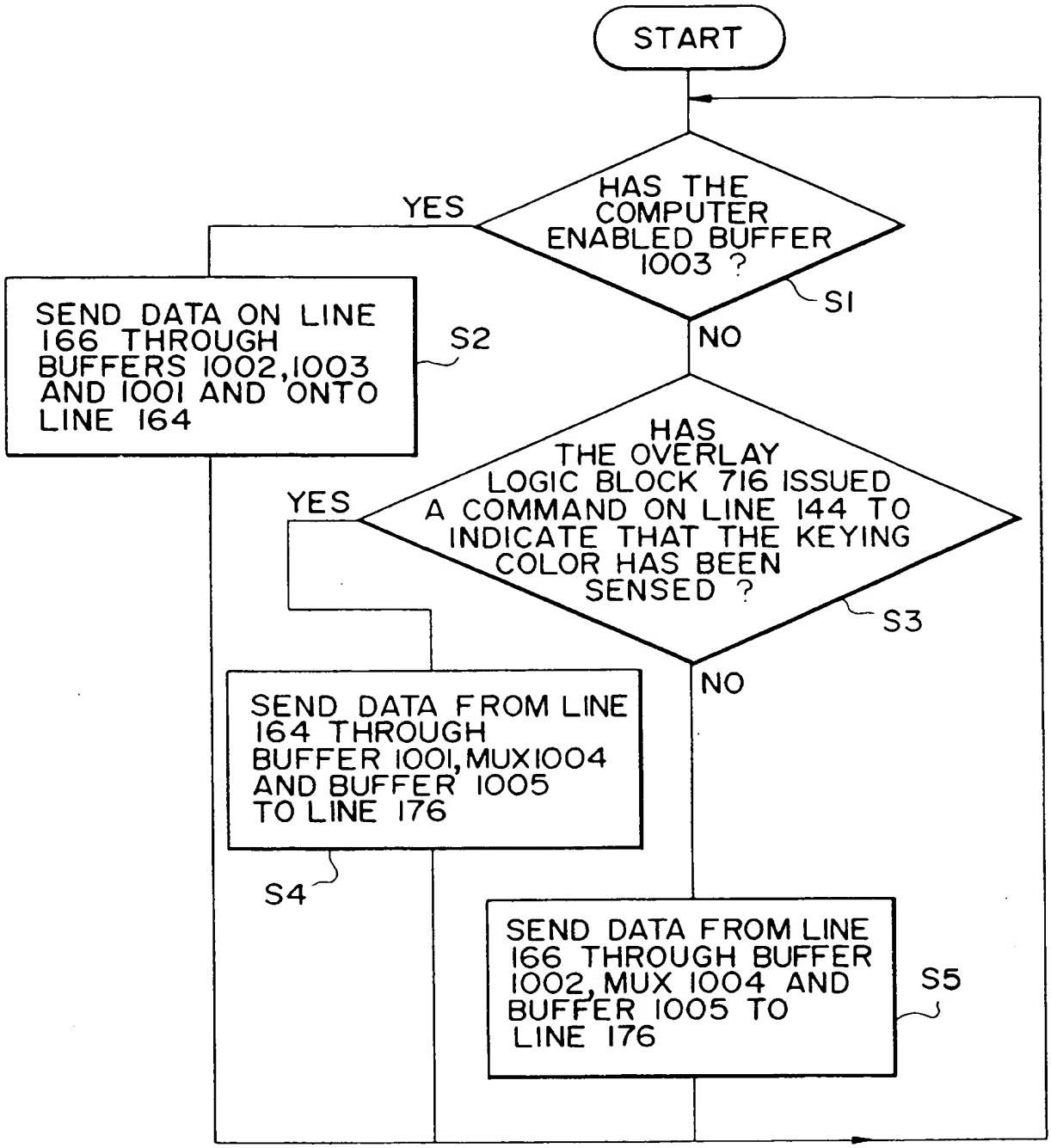
START
HAS THE COMPUTER ENABLED BUFFER 1003 ?
S1
YES
NO
SEND DATA ON LINE 166 THROUGH BUFFERS 1002,1003 AND 1001 AND ONTO LINE 164
S2
HAS THE OVERLAY LOGIC BLOCK 716 ISSUED A COMMAND ON LINE 144 TO INDICATE THAT THE KEYING COLOR HAS BEEN SENSED ?
S3
YES
NO
SEND DATA FROM LINE 164 THROUGH BUFFER 1001, MUX1004 AND BUFFER 1005 TO LINE 176
S4
SEND DATA FROM LINE 166 THROUGH BUFFER 1002, MUX 1004 AND BUFFER 1005 TO LINE 176
S5

FIG.12

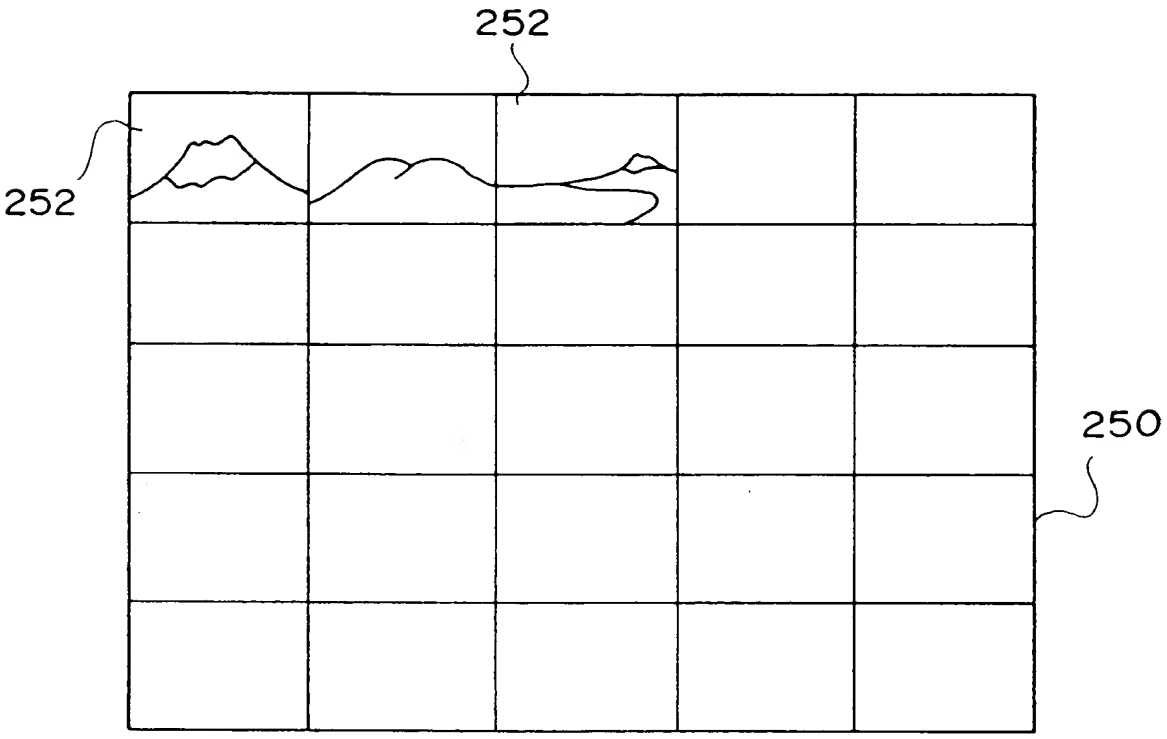

FIG.13

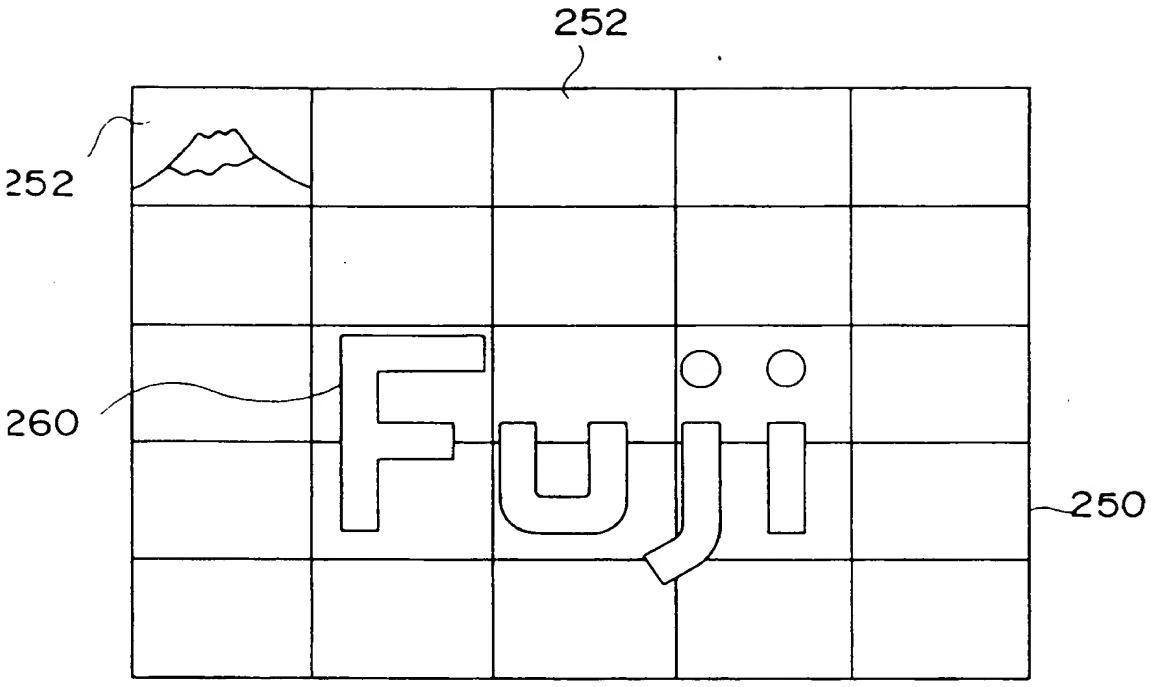

FIG.14

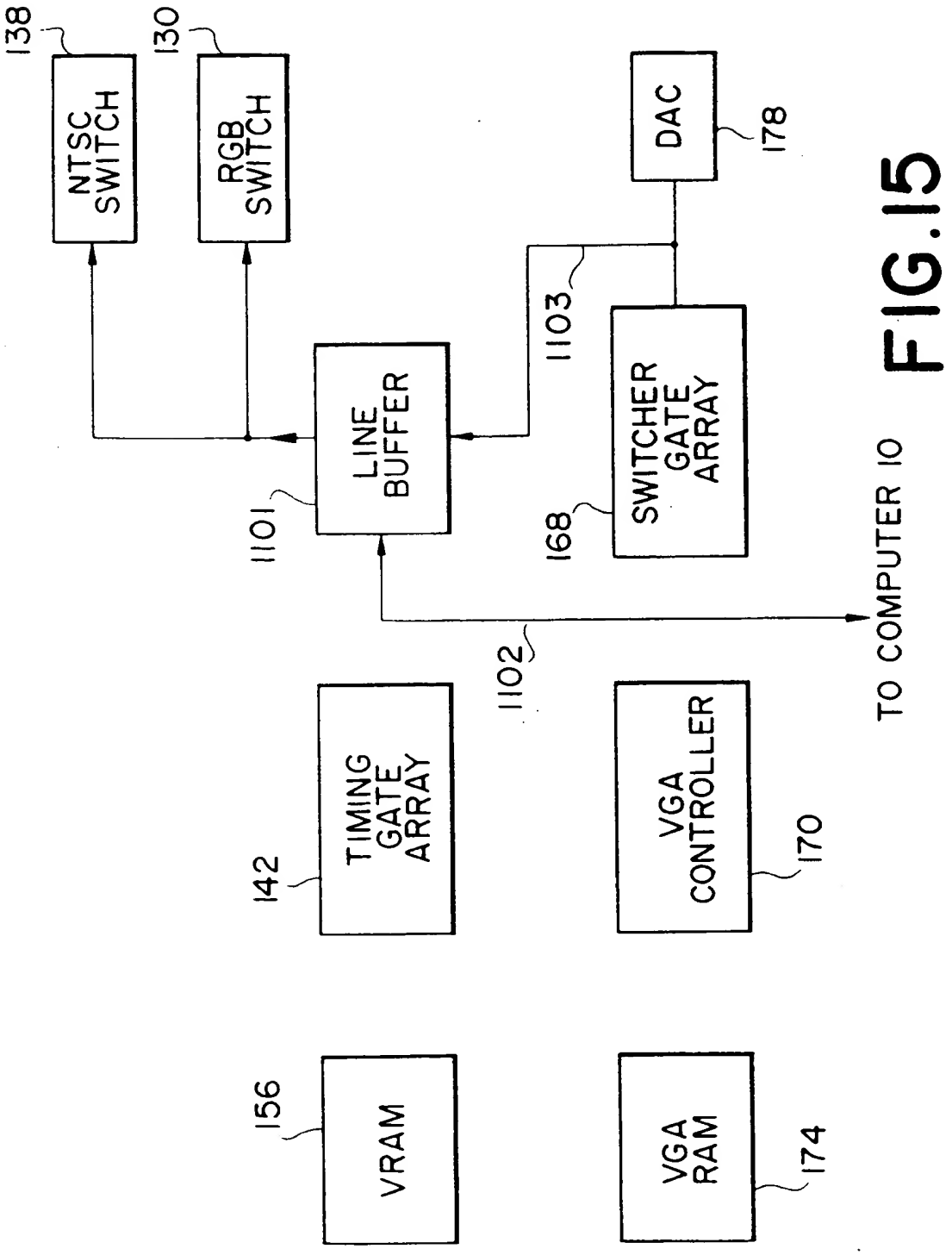
138
NTSC SWITCH
130
RGB SWITCH
DAC
178
1103
LINE BUFFER
1101
SWITCHER GATE ARRAY
168
TO COMPUTER 10
1102
142
TIMING GATE ARRAY
VGA CONTROLLER
170
156
VRAM
VGA RAM
174

FIG.15

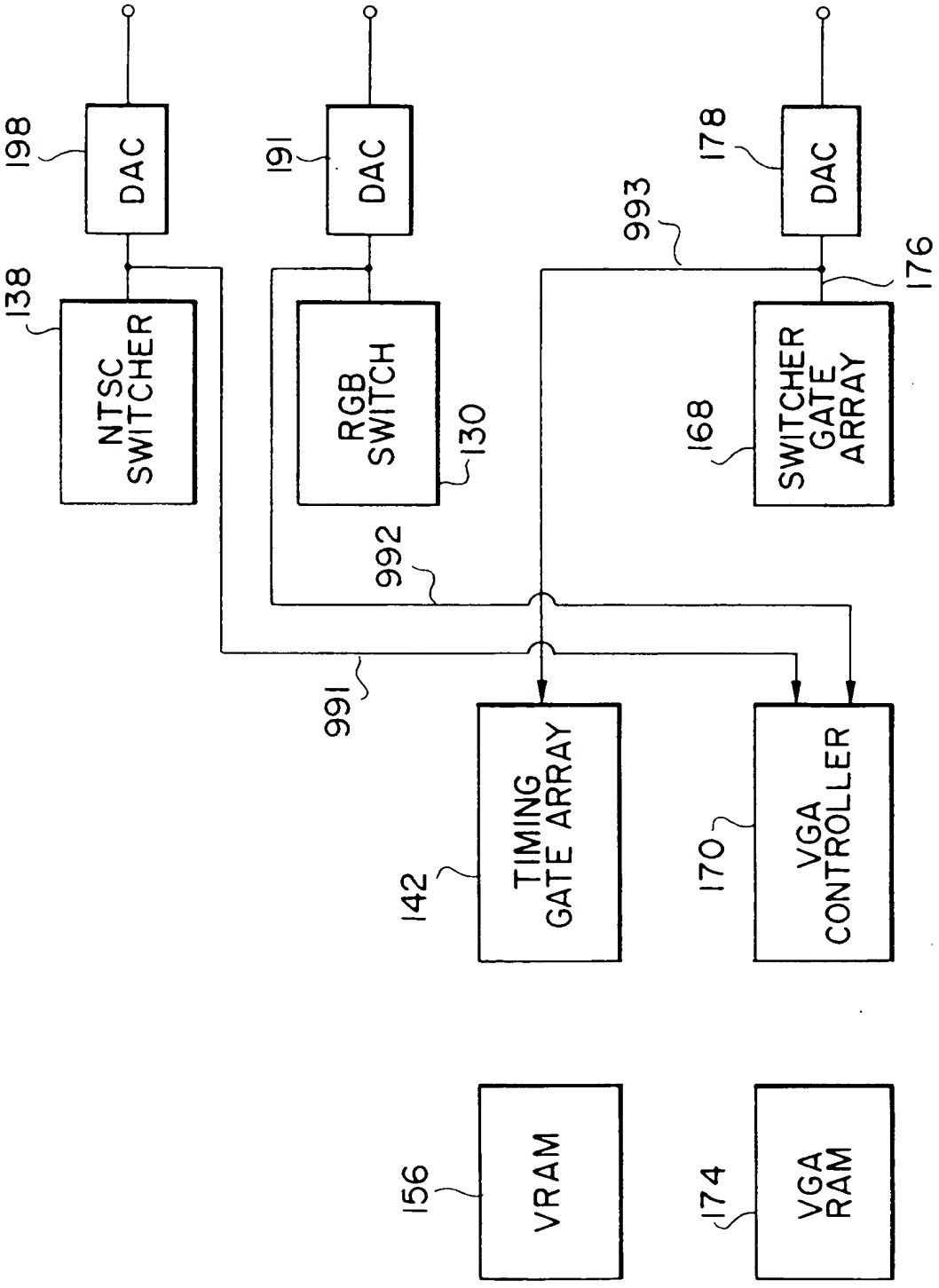
198
DAC
191
DAC
178
DAC
993
138
NTSC SWITCHER
RGB SWITCH
130
176
168
SWITCHER GATE ARRAY
992
991
142
TIMING GATE ARRAY
170
VGA CONTROLLER
156
VRAM
174
VGA RAM

FIG.16

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09.11.90 US 611201
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(88) Date of deferred publication of the search report:
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(74) Representative: **Patentanwälte Grünecker, Kinkeldey, Stockmair & Partner**
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(54) Image data processing apparatus.

(57) A video data processing apparatus converts one of NTSC type and VGA type video signals to the other or overlays the two types of video signals and outputs them as either an NTSC type overlaid video signal or a VGA type overlaid video sigal. The processing apparatus has two video memories (156, 174) for storing video signal data. One of the two video memories stores solely VGA type video data. The other video memory stores either VGA type video data or NTSC type video data depending upon the particular function being carried out by the processing apparatus. Video data may be read out from the other video memory using different scan rates so that an individually dedicated memory is not required for each type of video data in performing the above-mentioned conversions and overlays.

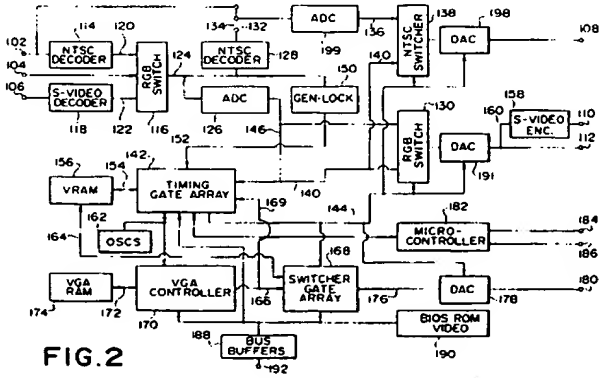

FIG.2

EP 0 484 981 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 11 9095

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 384 257 (INTERNATIONAL BUSINESS MACHINES) * the whole document *	1-11	H04N7/01 H04N5/76 H04N5/445 G11B27/32
A	US-A-4 730 260 (M.MORI ET AL) * the whole document *	1-4,10	G09G1/16 H04N5/262
A	EP-A-0 276 800 (IBP PIETZSCH GMBH) * the whole document *	1	
P,A	US-A-5 014 128 (B.W.CHEN) * column 2, line 25 - line 38 *	1,3,4,10	
A	EP-A-0 326 327 (SONY CORPORATION) * the whole document *	1-3,10	
A	WO-A-8 807 310 (DIGITAL EQUIPMENT CORPORATION) * the whole document *	1,3	
P,A	EP-A-0 419 814 (INTERNATIONAL BUSINESS MACHINES) * the whole document *	1,3,4,10	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H04N G11B G09G
P,A	EP-A-0 422 447 (KABUSHIKI KAISHA TOSHIBA) * column 73, line 31 - column 74, line 18 *	1,3	
A	EP-A-0 109 038 (WANG LABORATORIES INC.) * the whole document *	1,3,4,10	
A	EP-A-0 352 012 (INTERNATIONAL BUSINESS MACHINES) * the whole document *	1,4-7	
A	EP-A-0 320 300 (IDR INC.) * the whole document *	1-3	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 OCTOBER 1993	VERSCHELDEN J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

European Patent Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid,

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,

namely:

see sheet -B-

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid,

namely claims:

☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims:

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 11 9095

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	EP-A-0 454 414 (SONY CORPORATION) * the whole document *	1-3	
X	US-A-4 956 707 (OAKLEY D. ET AL) * the whole document *	14-17	
X	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS vol. 35, no. 3, 30 August 1989, NEW YORK US pages 624 - 628 , XP000065993 KOHIYAMA K. ET AL 'Development of a digital TV system for use in computer systems' * the whole document *	14-17	
P,X	EP-A-0 431 845 (RASTEROPS CORPORATION) * the whole document *	14-17	
P,X	EP-A-0 404 393 (INTERNATIONAL BUSINESS MACHINES) * the whole document *	14-17	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
E	EP-A-0 483 467 (GRAFITE S.R.L) * the whole document *	14-17	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 OCTOBER 1993	VERSCHELDEN J.

CATEGORY OF CITED DOCUMENTS

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L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-13 : An image data processing apparatus for processing image date representative of a real image or graphic image and used for overlaying the two former types of images.

2. Claims 14-17 : A memory system for use in an image data processing apparatus and used for data format conversion e.g. data type conversion and time base conversion.